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Why RISC-V Is Not Nearly Boring Enough

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When RISC-V grows up, it wants to be a wildly successful computing platform. Being an ISA is fun but being the world's fastest supercomputer would be really cool.

So how do we get there? By being dead boring. If I have an operating system to install on a platform built around the RISC-V ISA, the install *MUST* work out of the box – no mucking about with strange boot loaders, or grabbing odd bits of firmware and kernel patches. To do that means standardizing what a RISC-V platform looks like so that an OEM knows exactly what must be built, and so that an operating system knows what exactly what hardware and firmware it will find.

And let's just say that right now, the RISC-V Platform Specification has a long way to go to. An OEM can only guess at what needs to be built; an OS can only run by using a lot of fiddly bits. These are some of my thoughts on what needs to be done:

. A clear vision
. A clear process
. A clear – and complete – specification

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