Enabling 8K displays

A story of 33M pixels, 2 CRTCs and no Tears!

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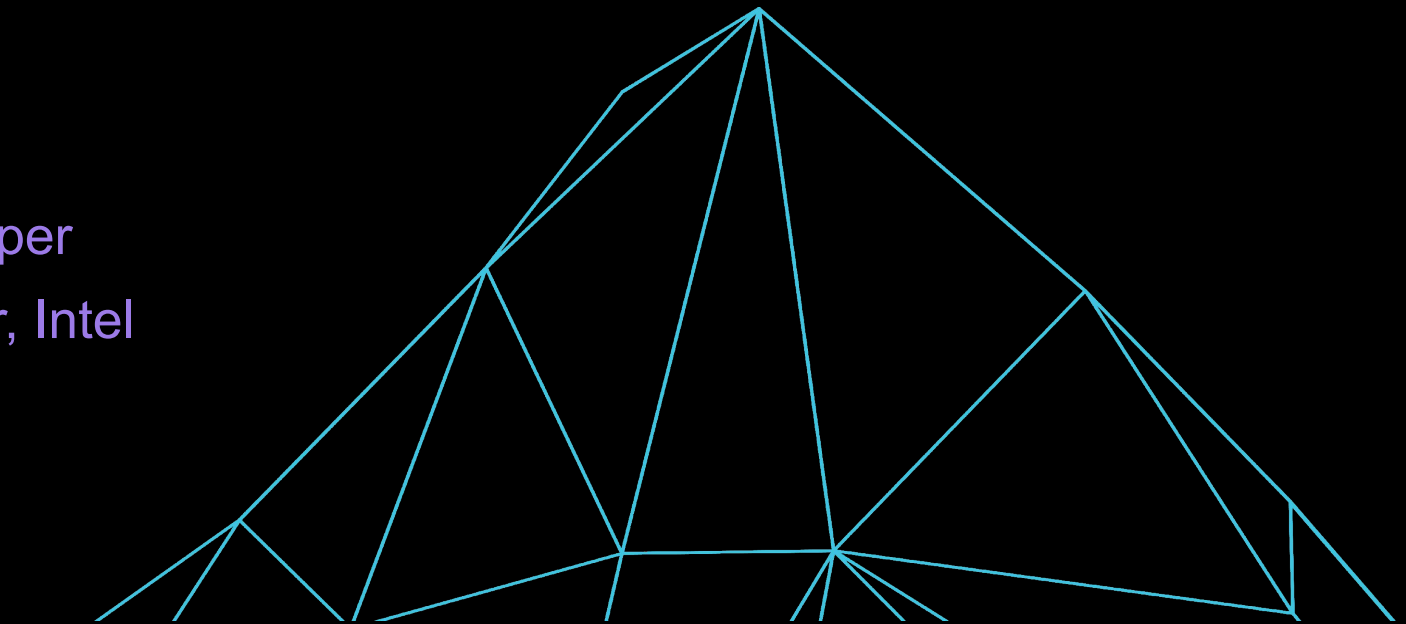
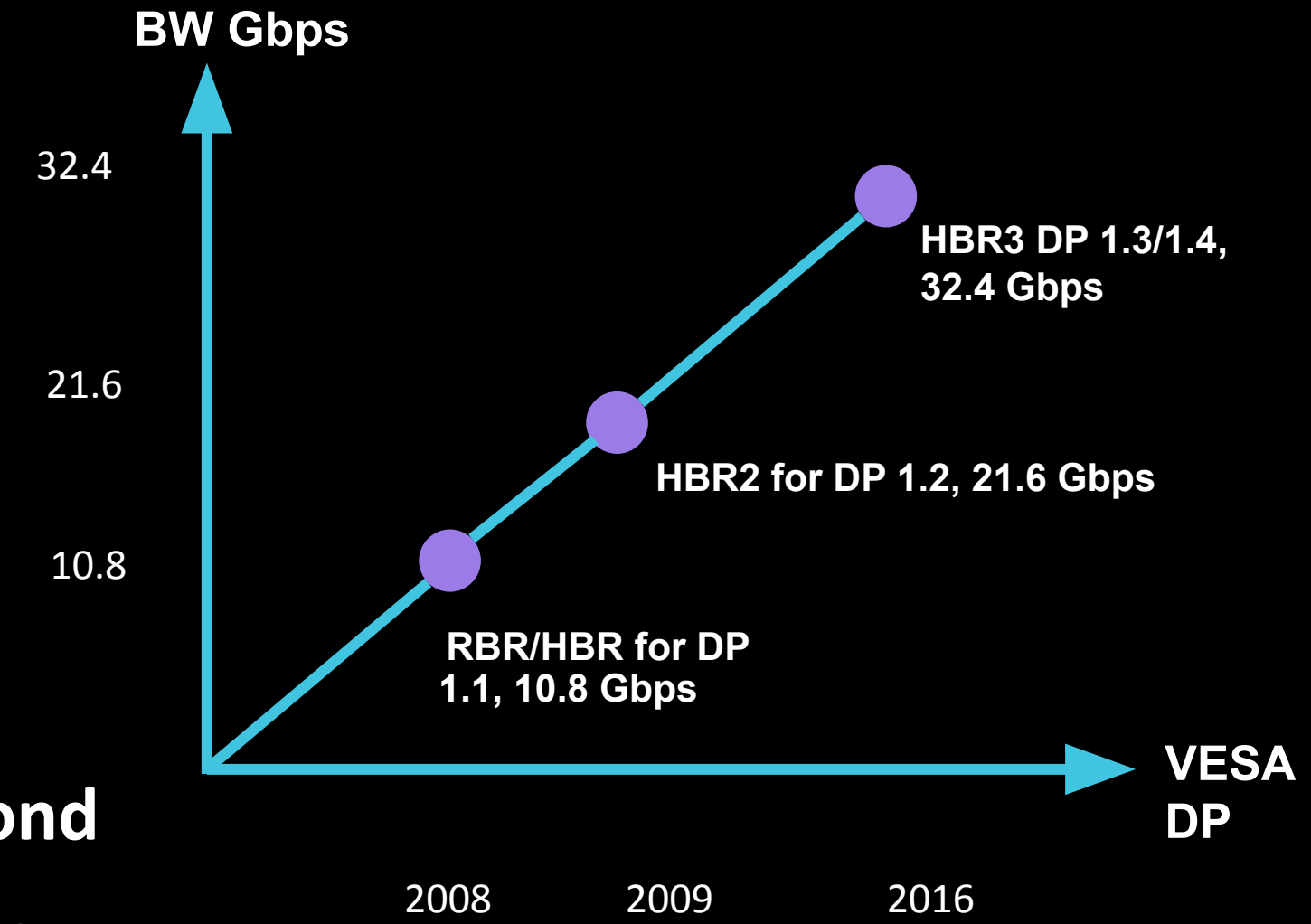


8K BW vs. DP BW



33 M Pixels/ **Frame**

8K@60: 1980 M Pixels / **Second**

Total Display BW : 48 G Bits/sec

Can we stream 8K using single DP connector yet?

Required Display BW for 8K@60

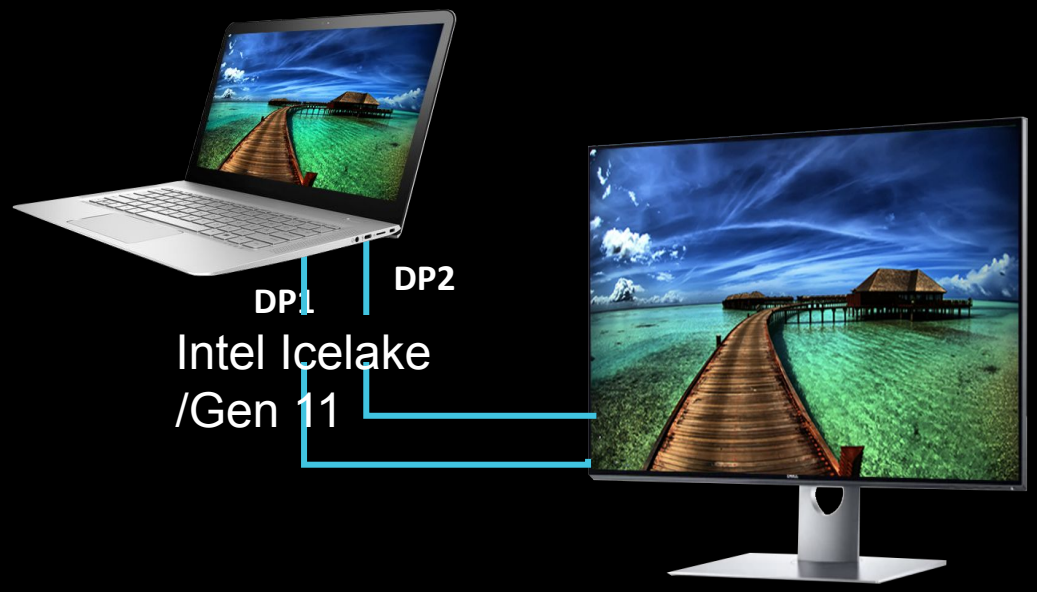
>=48 Gbits/sec

Available BW of DP @ HBR3

32.4 Gbits/sec

X

Output 8K using 2 DP connectors



Need for 2 CRTCs/Pipes on Intel HW

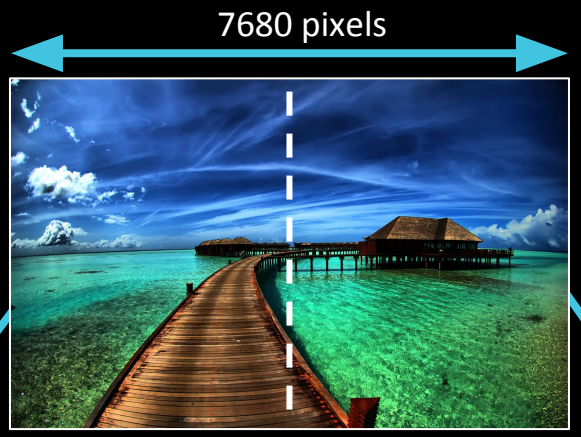
- Display BW should fit within Maximum Pipe Pixel Rate

- Max Pipe Pixel Rate = 2 * CDCLOCK
  - Max CDCLOCK on ICL = 652MHz
  - With 99% clock usability, max Pixel clock = (2 * 990 * 652)/ 1000 = 1290 MHz

- For 8K@60, Pixel Clock = 2200 MHz

* Split 8K@60 across 2 CRTCs/ 2Pipes

Enable 8K in Dual Pipe Dual Port Configuration



8K Tiled Display

Parsed from Monitor's DisplayID EDID data

3840 pixels

Left Display Pipe/Port

Tile 1
3840 x 4320
DP link BW ~ 24Gb/s

3840 pixels

Right Display Pipe/Port

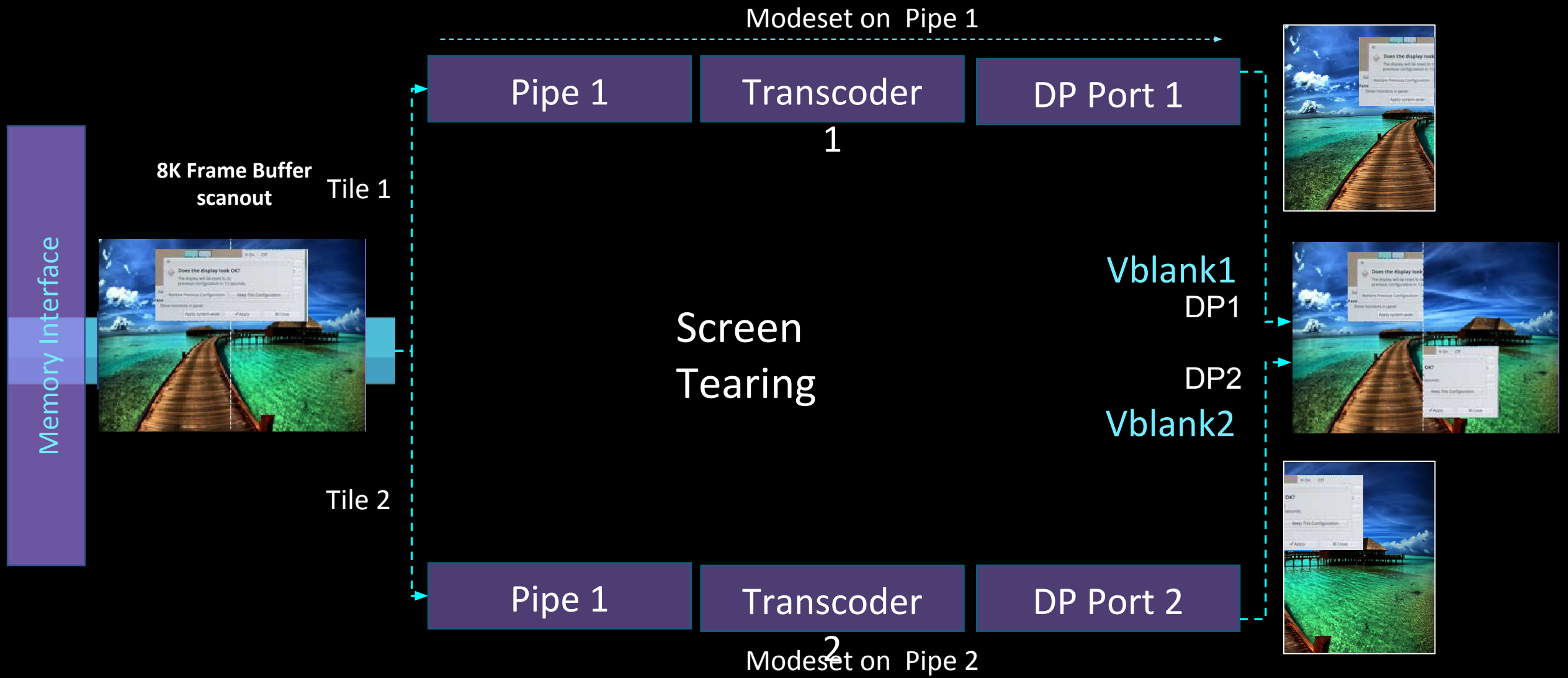
Tile 2
3840 x 4320
DP link BW ~ 24Gb/s

DP 1 @ 32.4 Gbps

DP 2 @ 32.4 Gbps

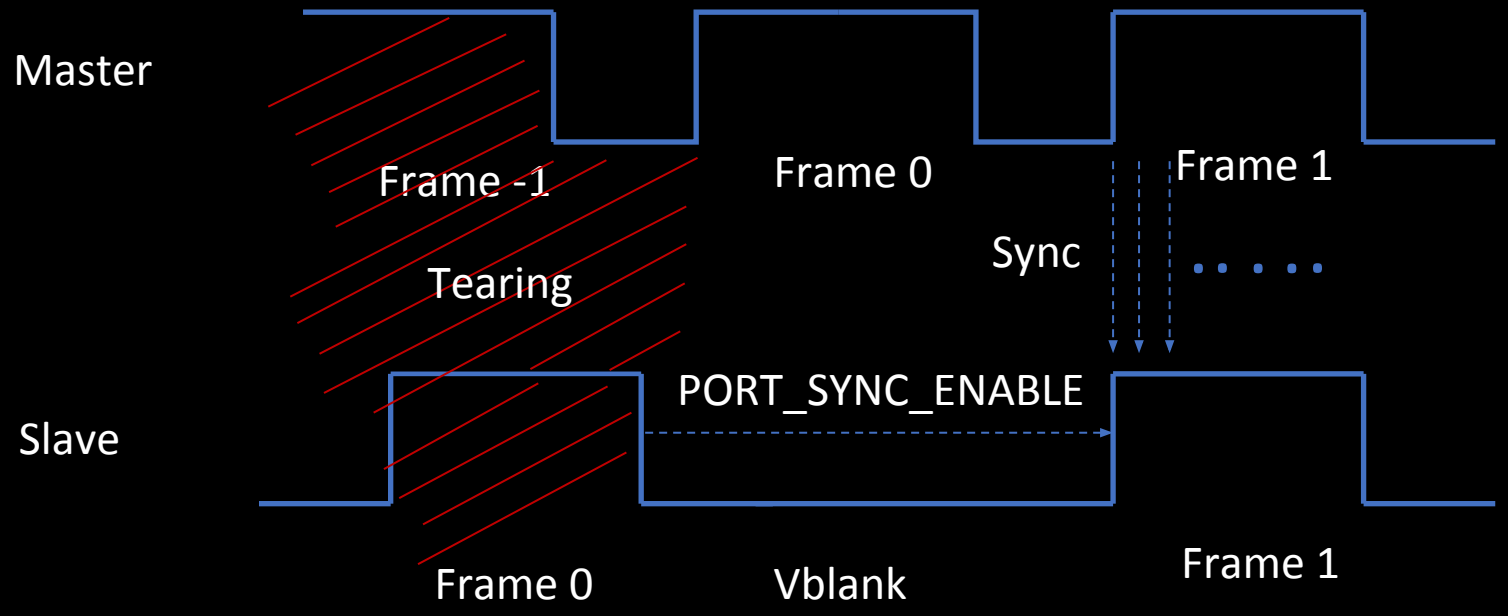
Final 8K Display

Challenges with 2 CRTCs 2 PORTS



Solution: Transcoder Port Sync

- PORT SYNC mode forces two or more transcoders involved in tiled modeset to be in sync
- Only enabled in the slaves, HW lock-steps slave timings with the master



Atomic Check

Atomic Commit

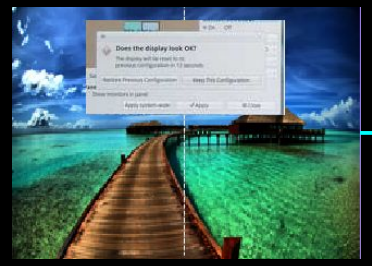
PIPE B/ CRTC 1

Master Transcoder B

Port B

Output next frame

8K Frame



Last tile = master
Master crtc_state
Slave_bitmask = BIT(PipeA)

First tile = slave
Slave crtc_state
master_trans = PipeB

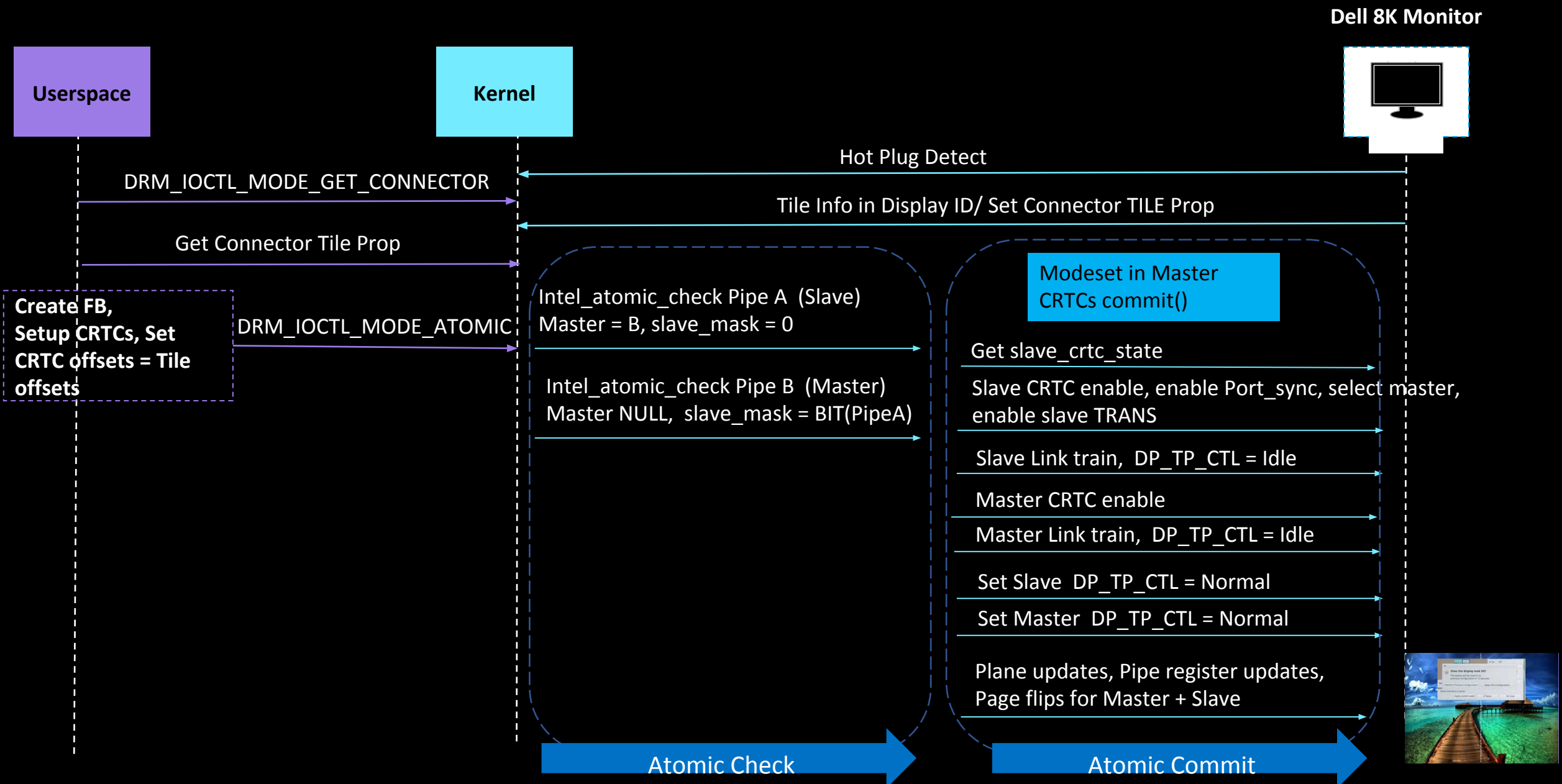
Enable Port Sync Mode
Set Master select

PIPE A/ CRTC 0

Slave Transcoder A

Port A

Atomic KMS changes



Synchronized page flips validation/CI

- IGT test kms_dp_tiled_display.c and TILE property parser to decode the tile information added to igt/lib/igt_kms.c
- Validate by capturing page flip event timestamps on each CRTC and ensuring they are within 10us (credits: Madhumitha, Simon Ser)

```
(kms_dp_tiled_display:4883) DEBUG: Page Flip Event received from
CRTC:91 at 91:650485
(kms_dp_tiled_display:4883) DEBUG: Page Flip Event received from
CRTC:152 at 91:651078
(kms_dp_tiled_display:4883) CRITICAL: Test assertion failure
function page_flip_handler, file kms_dp_tiled_display.c:353:
(kms_dp_tiled_display:4883) CRITICAL: Delayed page flip event from
CRTC:152 at 91:651078
```

Screen Tearing, Delayed page flips on second tile

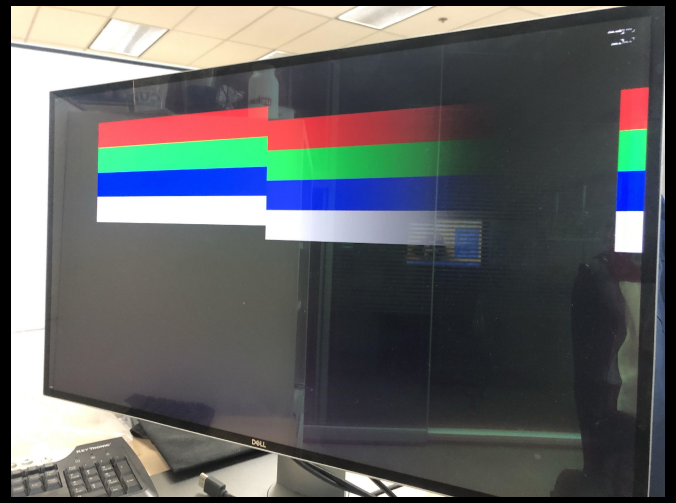
```
(kms_dp_tiled_display:11227) DEBUG: Page Flip Event received from
CRTC:91 at 437940:10356
(kms_dp_tiled_display:11227) DEBUG: Page Flip Event received from
CRTC:152 at 437940:10355
```

Synchronized Flips, within 1us

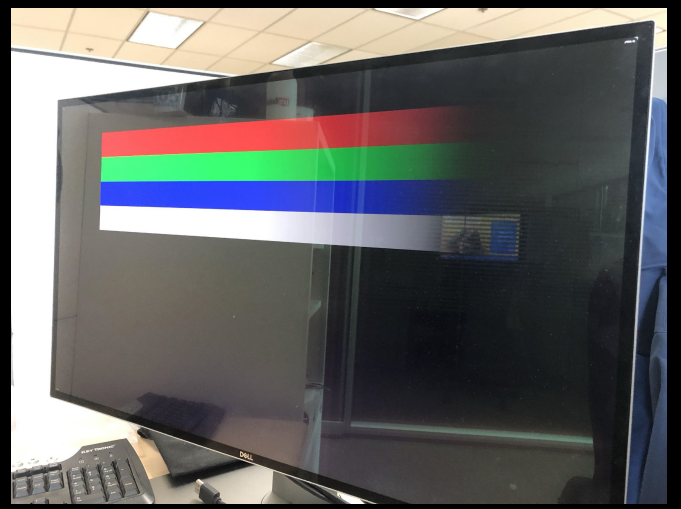
8K Results with PORT SYNC

- Support for transcoder port sync and dual pipe dual port 8K tiled display to land in 5.4.0 Linux Kernel

TEARING



8K Output with PORT SYNC



Questions?

Thanks to the entire Intel-gfx and dri-devel community!!

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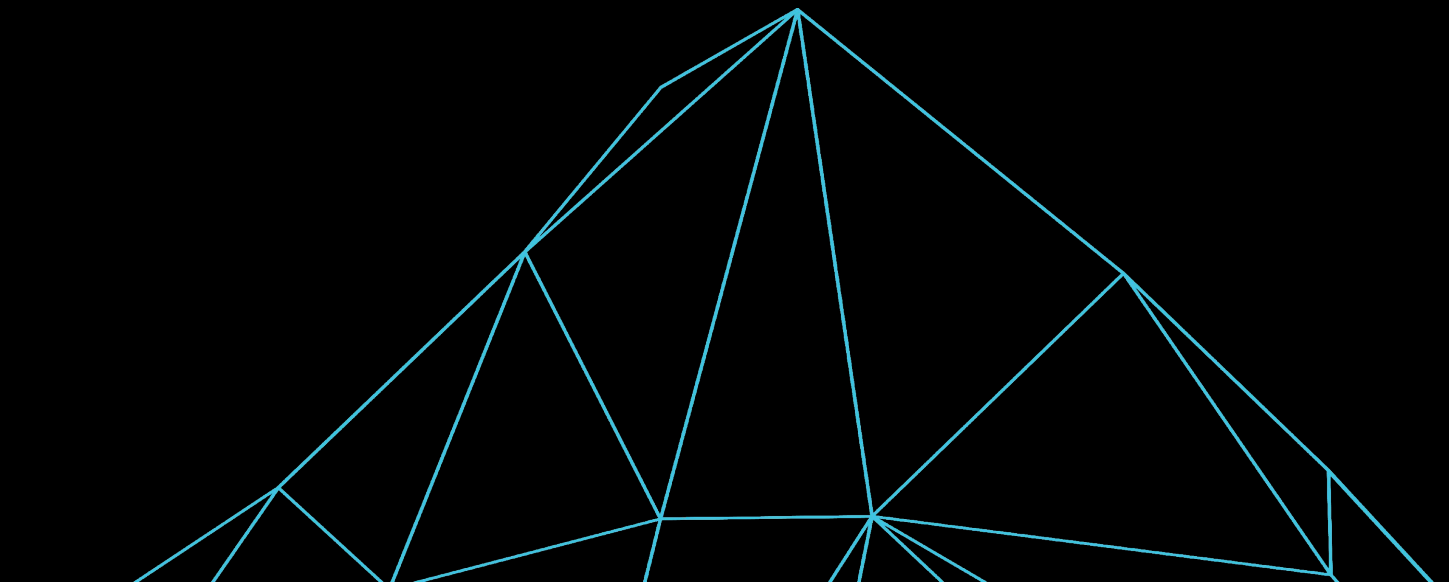

Acknowledgements

- Big thanks to Matt Roper, Jani Nikula, Ville Syrjala, Maarten Lankhorst, Daniel Vetter for their kernel code feedback and reviews

- Thanks to our intern Madhumitha Tolakanahalli for implementing the IGT and Simon Ser and Petri Latvala for IGT reviews

- Thanks to the entire Intel-gfx and dri-devel community