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Reuse host JIT back-end as offload back-end

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eBPF offload is a powerful feature on modern SmartNICs used to accelerate XDP or TC based BPF. The current kernel eBPF offload infrastructure was introduced for the Netronome NFP based SmartNICs, these were based around a proprietary ISA and had some specific verifier requirements.

In the near future this may be joined by SmartNICs using public ISA's such as RISC-V and Arm which also happen to be used as host CPUs. This talk will discuss the implications of reusing these ISAs and other back-end features for offload to a sea of cores as well as how much of a host CPU back-ends can be reused and what additional infrastructure may be needed. As an example we will use the current work on a many core RISC-V processor ongoing within.

I agree to abide by the anti-harassment policy

Yes

Primary author: Mr WANG, JIONG (Netronome Systems)

Presenter: Mr WANG, JIONG (Netronome Systems)

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