

Speaker's summary of the talk and discussion

Written by Guodong Xu, Qualcomm LPC26 RISC-V Microconference, Prague, 6 October 2026.^{1,2}

Disclaimer: not official minutes.

This is a summary of my talk and the discussion around it. I appreciated the lively exchange of views during the session and am pleased to see the follow-up work already underway, with at least three related patch series posted to the mailing list.

Patch status is updated as of 10 October 2026.

1. The four asks and responses

Ask 1: Does the rva23u64 bit make sense?

The proposed rva23u64 bit would report profile support. Two review points remain for the core patches: use “supports RVA23” semantics, with corresponding RVA22 and RVA20 bits so glibc can fall back through profiles; and explicitly document that the bit does not inherit the historical implicit behavior associated with the IMA bits.

On 9 October, Paul Walmsley picked up the first eight of v8's eleven patches into `riscv/for-next`. The three core patches remain for v9.^{3,7} I will send v9 soon and address the community's concerns in it.

Ask 2: Can profiles guide library selection?

The request is for distros to ship RVA23U64 builds of selected libraries once the kernel bit lands. Peter Bergner reiterated the proposed glibc approach: select profile-based library builds through glibc-hwcaps using kernel profile bits. IFUNC would still handle microarchitecture-specific choices. No commitment from a distro to ship these builds was recorded.

Ask 3: Should we deprecate disabling V?

Dynamically disabling V can undermine the assumptions behind library dispatch. Paul Walmsley supported deprecation on the condition that no existing users depend on the interfaces; no such users were identified in the session. Samuel Holland posted a three-patch deprecation series on 7 October.⁴

Ask 4: What about future stateful extensions?

The question concerns extensions that introduce register state, such as matrix extensions. No detailed design was established in the session. Samuel's subsequent cover letter states that there is no plan to add similar user-space disabling controls for future stateful extensions, including matrix extensions.⁴

2. Related follow-up patch series

Reporting only usable extensions

Radim Krčmář, Qualcomm. Six-patch series: “riscv: hwprobe: do not report disabled extensions”.⁵

Addresses incorrect extension reporting through hwprobe, including Zfa and Zcd being reported on harts without an FPU. Status: posted series.

Simplifying cpufeature macros

Conor Dooley, Microchip. RFC to simplify the cpufeature macros used to represent extension groupings.⁶

Proposes removing `RISCV_ISA_EXT_BUNDLE` from cpufeature and retaining `SUPERSET`. This is relevant to representing the B extension in the RVA23 series. Status: RFC.

Deprecating the controls for disabling V

Samuel Holland, SiFive. Three-patch series posted on 7 October.⁴

Proposes deprecating the `prctl` and `sysctl` interfaces that let user space dynamically disable V. This is the implementation follow-up to Ask 3. The cover letter also states that similar controls are not planned for future stateful extensions. Status: posted series.⁴

References

1. Session: <https://lpc.events/event/20/contributions/2626/>
2. Original slides: <https://lpc.events/event/20/contributions/2626/attachments/1995/4541/lpc26-rva23-in-practice-v3-2026-10-02.pdf>
3. Patchwork notification: <https://lore.kernel.org/all/179157660809.984023.2184718764665109991.git-patchwork-notify@kernel.org/>
4. Samuel Holland: cover letter: <https://lore.kernel.org/all/20261007085126.222688-1-samuel.holland@sifive.com/>
5. Radim Krčmář: series: <https://lore.kernel.org/all/20261006075303.205216-1-radim.krcmar@oss.qualcomm.com/>
6. Conor Dooley: RFC: <https://lore.kernel.org/all/asUa6pJVpXb2EadB@squawk/>
7. RVA23U64 hwprobe v8: <https://lore.kernel.org/r/20260920-rva23u64-hwprobe-v2-v8-0-5f14bc5c23d3@oss.qualcomm.com>