



Dynamic Runtime Prediction of CPU Idle-State Exit Latency

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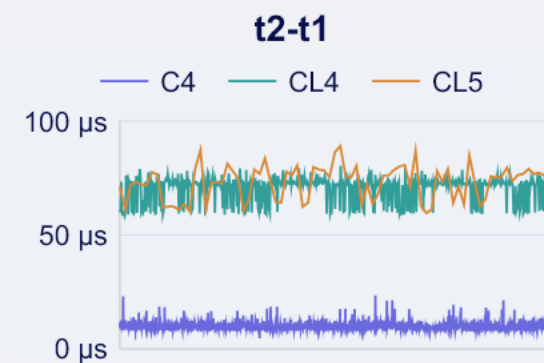
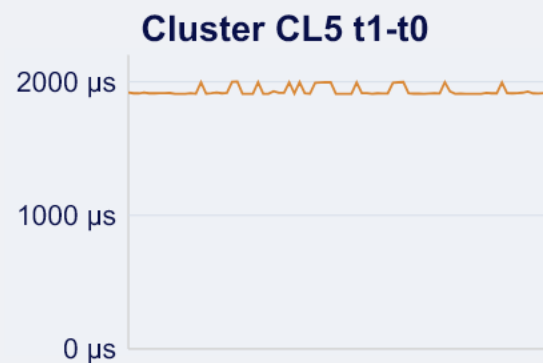
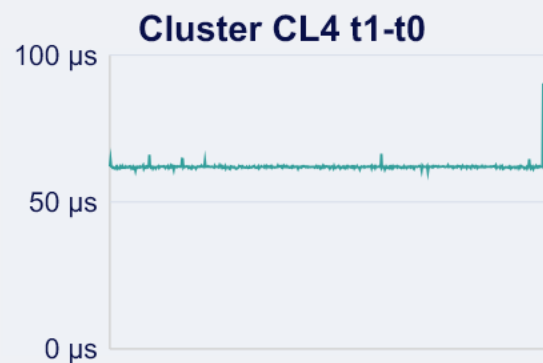
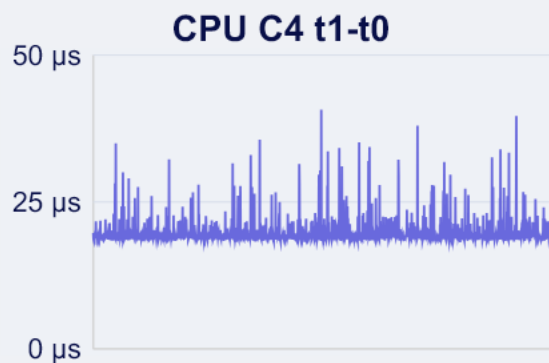
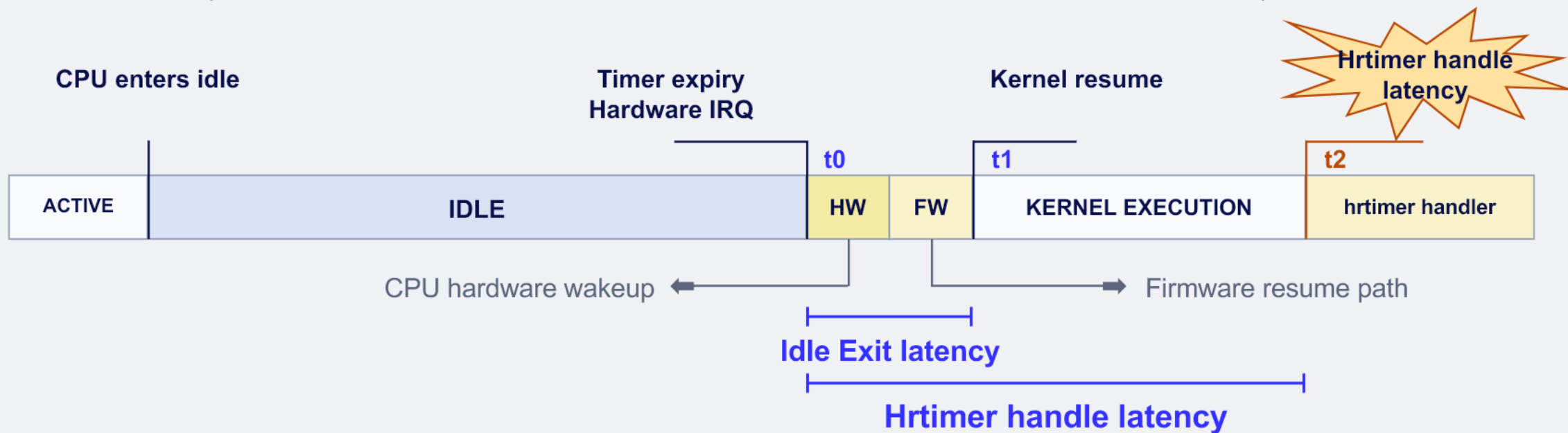
Qualcomm CSE Linux kernel team

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Idle Exit Latency and hrtimer handle latency

Hardware wakeup, firmware resume, and kernel execution all add to the hrtimer handle latency.



Measuring CPU and Cluster Idle Exit Latency

Record at kernel resume. Keep separate CPU and cluster histories for idle exit latency.



● CPU sample

Exit latency = $t_1(A) - t_0(A)$

Records: CPU ID + actual idle level

Valid sample: timer expired AND

only the timer IRQ is pending

◆ Cluster sample

Exit latency = $t_1(B) - t_0(B)$

Records: cluster ID + actual level

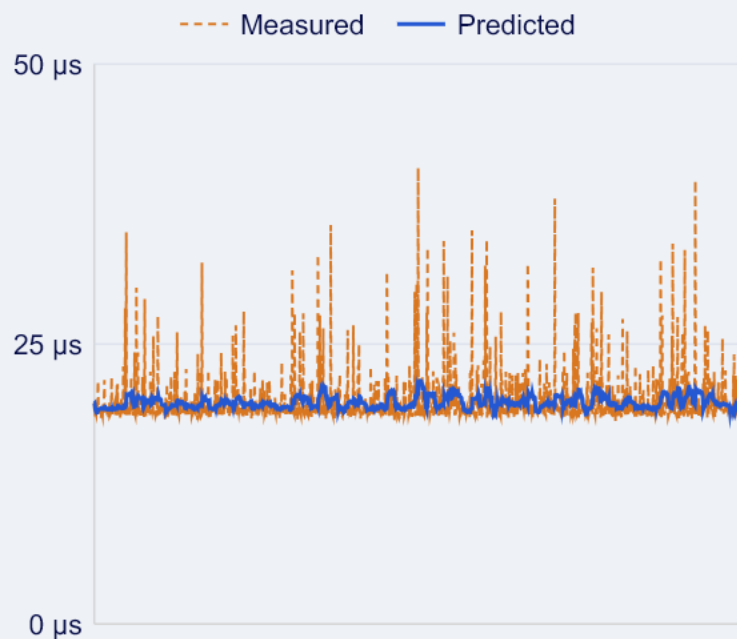
CPU sample conditions, plus:

No non-timer IRQ on other CPUs

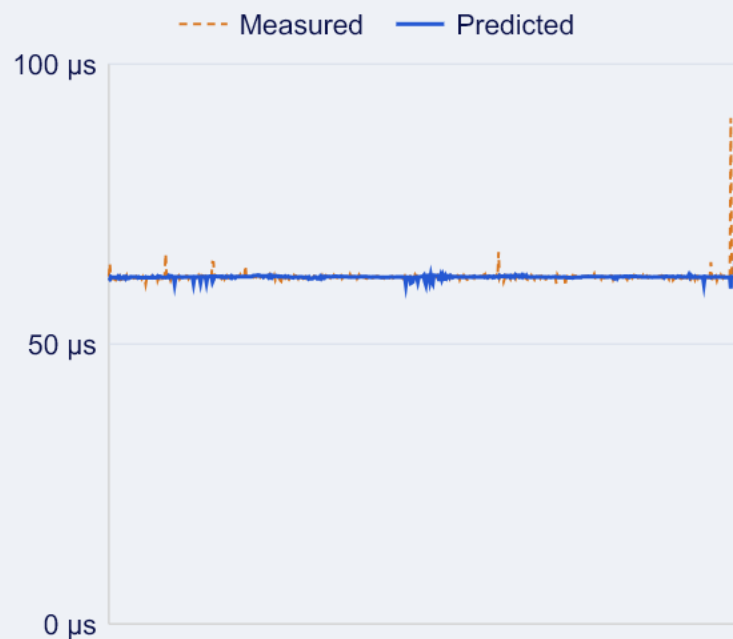
Prediction by History Window: Idle Exit Latency Data

Valid samples → Sliding window → Mean → Prediction

CPU C4



Cluster CL4



Cluster CL5

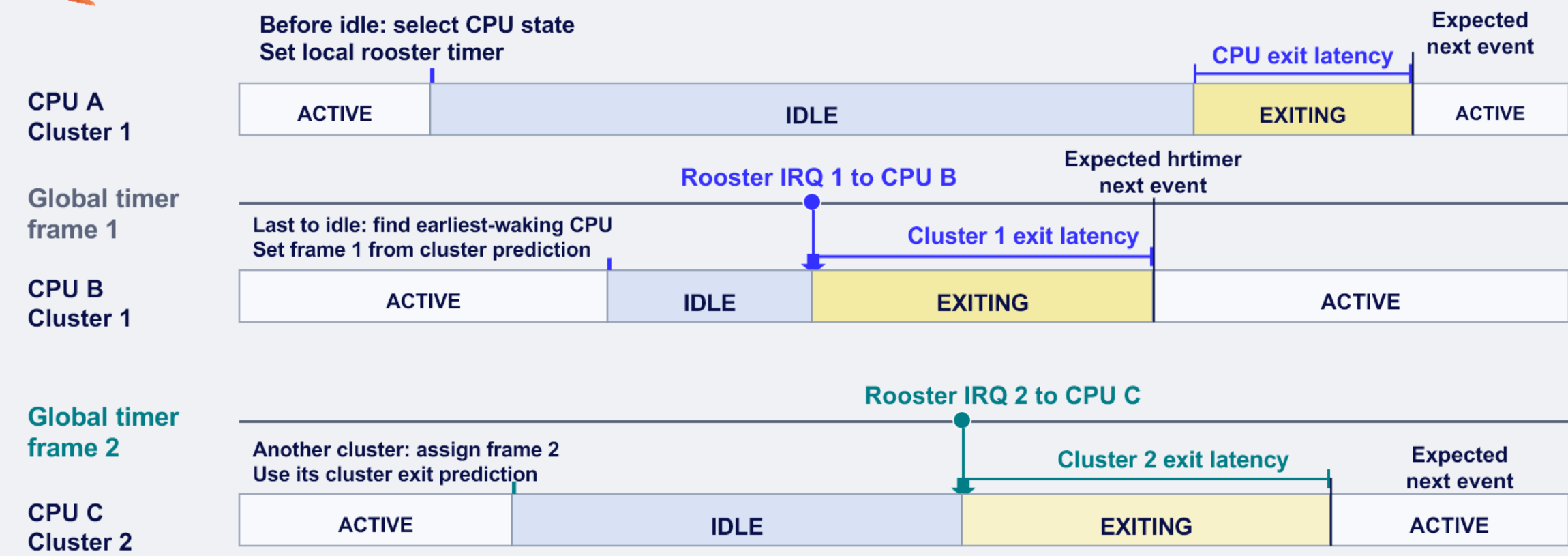


Hrtimer Compensation: idle Exit latency

Each cluster has its own Rooster timer IRQ.



Rooster IRQ time = hrtimer next event – predicted idle exit latency



Each frame: rooster IRQ = next event – cluster exit latency

Hrtimer Compensation: idle Exit latency

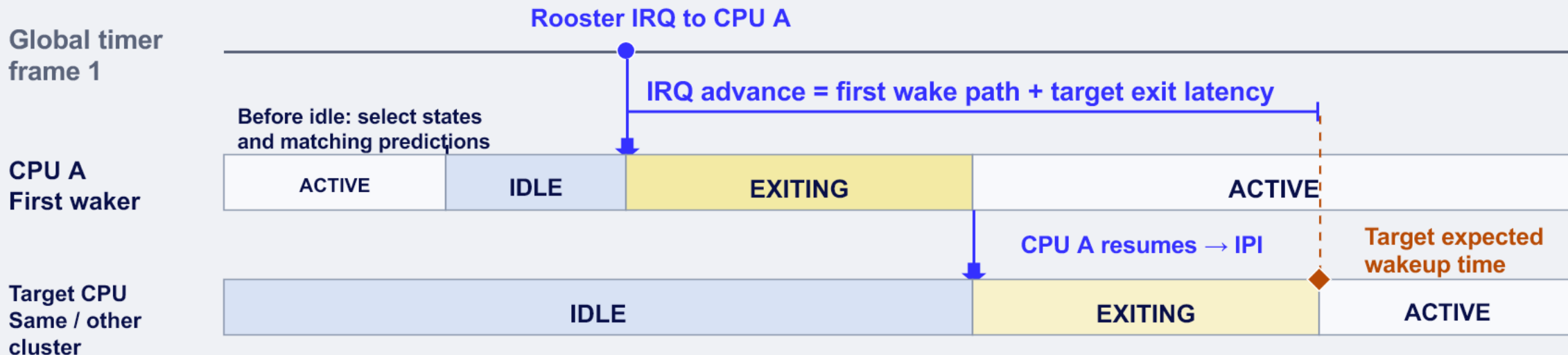
One Global Rooster timer IRQ + Rooster IPI.

Local arch timer stops in idle

Last CPU to idle programs the global timer.
CPU A forwards wakeups by IPI.

Multiple clusters share one global timer

Wake one CPU in the first cluster,
then send IPI to the other cluster.



Arch timer stops:

Cluster exit latency + target CPU exit latency

One timer across clusters:

Cluster 1 exit latency + cluster 2 exit latency

CPU Execution Timing After Rooster Compensation

Rooster IRQ advances HW/FW recovery so the kernel resumes near the original deadline.



Absolute mean (μ s)

Idle level	CPU C4	Cluster CL4	Cluster CL5
Before compensate t1-t0	19.824	61.991	1929.767
After compensate t1-t0	0.073	0.191	10.738

Open discussion

- Potential performance and real-time benefits?
- Rooster IPI overhead and power consumption?
- QoS implications?
- Use predicted idle exit latency for CPU idle-state selection?

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Thank You

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