



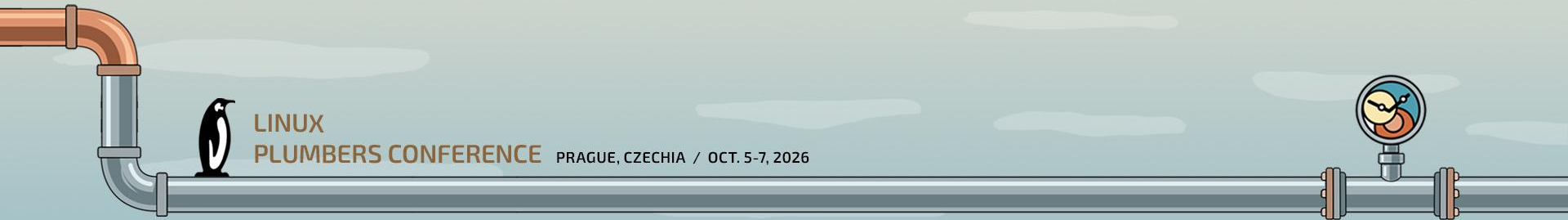
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Power Sequencing for Enumerable Busses - What's Next?

Chen-Yu Tsai

- Works on ARM-based Chromebooks at Google
- Current maintainer of wireless-regdb project
- Maintainer of Allwinner SoC within the kernel on the side



Enumerable Busses - Recap

- Devices can be "enumerated" directly by the host controller without additional hardware descriptions, provided they are operational.
- Making the device "operational" might require additional setup
- SD/MMC/SDIO (working)
- PCIe (working)
- USB
 - onboard devices can power on
 - no port power integration
 - no USB connector integration
- MDIO
 - reset GPIO only



M.2 USB Support

- Currently at v9 [\[1\]](#)
- Links USB ports to M.2 USB endpoints (and potentially USB A connector endpoints) using pwrseq API
- Needs reviews from USB maintainers
- Potential users
 - MediaTek Chromebooks
 - Qualcomm platforms
 - any device with M.2 WiFi
- USB A connector done but not sent [\[2\]](#)
- Can we also support onboard devices?



Power Control Platform Devices

- PCI and USB create sibling platform devices whose sole purpose is to handle power sequencing
- MMC gets power control platform devices from pwrseq nodes
- PCI and MMC both have custom ops
- Can these be made more generic and shared?
- Can we also use them for MDIO bus devices?



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Driver Core or Bus Integration

- Create power control platform devices in bus code
 - Already done for PCI
 - Similarly for USB
 - Bus-specific, probably not suitable for driver core
- Retrieve and toggle power sequencers in driver core or bus code during device instantiation?
 - Power sequencing interleaved with other driver controls, probably hard to separate



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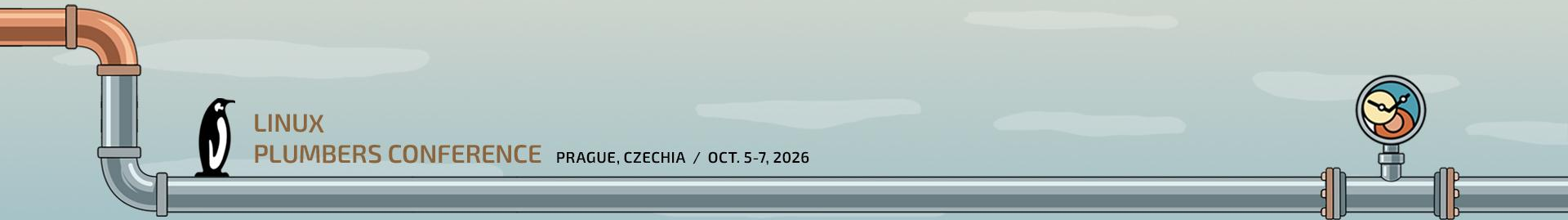
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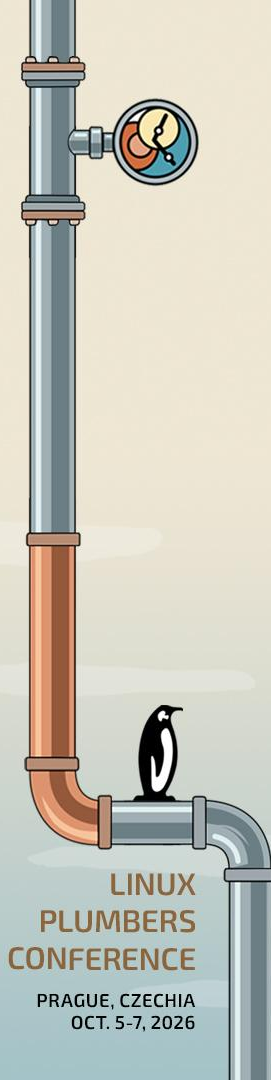


MDIO - Ethernet PHYs are mostly Trivial

- One or two power supply inputs
 - One clock input
 - One reset GPIO
 - One interrupt pin
- One trivial platform stub driver to put trivial PHYs in operating state?



Issues Along The Way

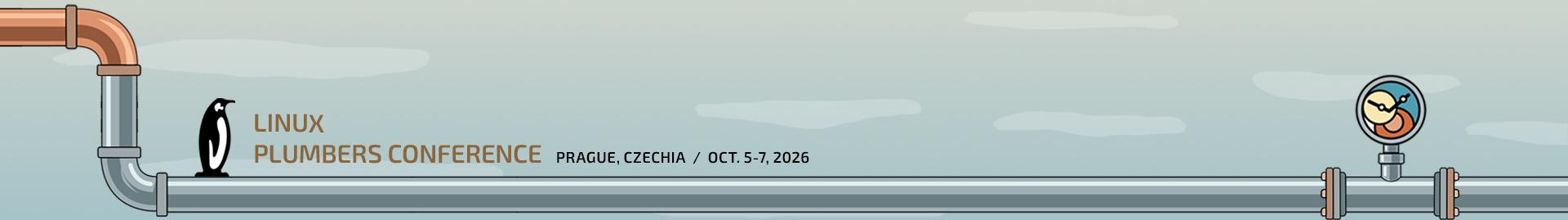


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Pwrseq Subsystem Limitations

- No fine control of power state
 - On & Off only
- Power sequencer matching and retrieval very free form
 - -EPROBE_DEFER only; no -ENODEV
 - Indefinite wait
 - Consumer side ends up with extra code to check for sequencer

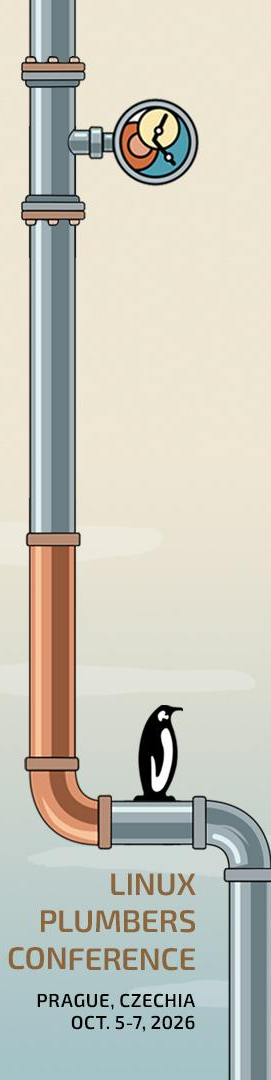


XHCI oddities

- has two root hubs (HS and SS)
- has a number of downstream HS and SS ports separately tied to the root hubs
- USB core does not consistently handle root hub port number to raw port number mapping
- Child USB device creation maps it correctly (to get the right child fwnode)
- USB port device does not
- Patches on the way



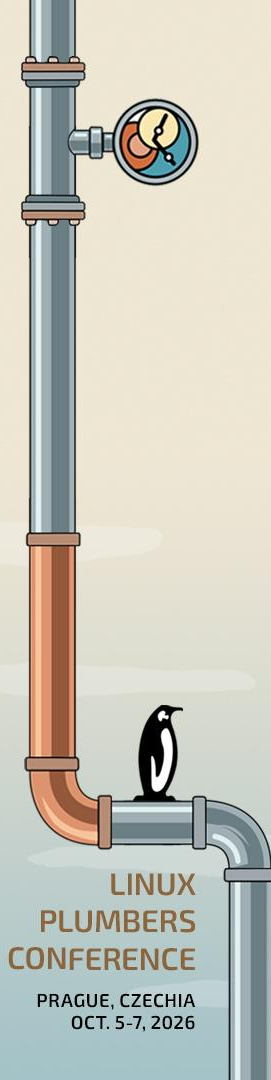
Thank you



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Backup Slides

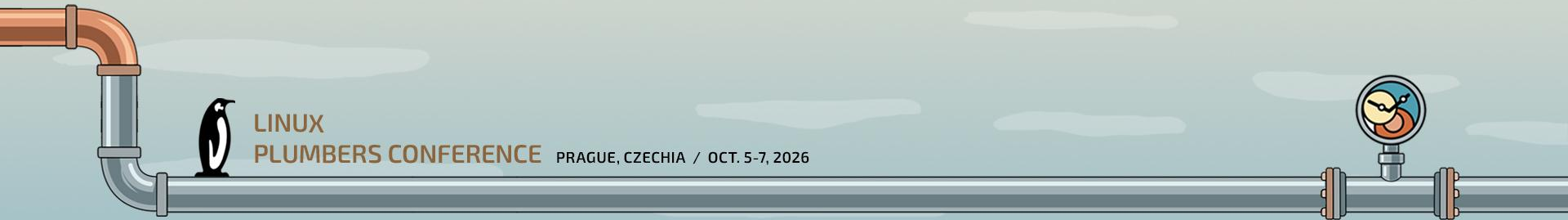
A vertical pipe with a pressure gauge and a penguin perched on a horizontal section. The pipe is blue with orange joints. The pressure gauge is circular with a yellow face and blue and red markings. The penguin is black and white, standing on a horizontal section of the pipe that curves downwards.

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SD / MMC / SDIO

- MMC-specific power sequencing bindings exist
- Bindings can't be changed
- MMC-specific pwrseq drivers work
- Subsystem maintainer prefers to keep them as is



USB

- USB connector and onboard device bindings exist
- Other external resources declared ad hoc
- VBUS regulators described as PHY supplies
- GPIOs tied to USB hosts or PHYs
- Host or PHY drivers enabling external resources for devices
- onboard USB devices have extra platform device, power sequencing not fully integrated with USB core
 - it turns on, that's it



PCI / PCIe

- PCI slot description covers standard PCI devices
- M.2 slot binding for E-key and M-key slots
- PCI pwrctrl mechanism handles PCI root, bus, switches
- Separate integration needed for each PCI host controller driver



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MDIO

- net maintainers don't want more ad hoc changes to enable a supply or a GPIO
- Request folks use `"ethernet-phy-id*"` compatibles
- Or make firmware do setup
- Not exactly "enumerable" if the ID is fixed in the DT
- Device vendors have changed components midway without identifiable change to board or firmware
- Firmware might not be updateable

