



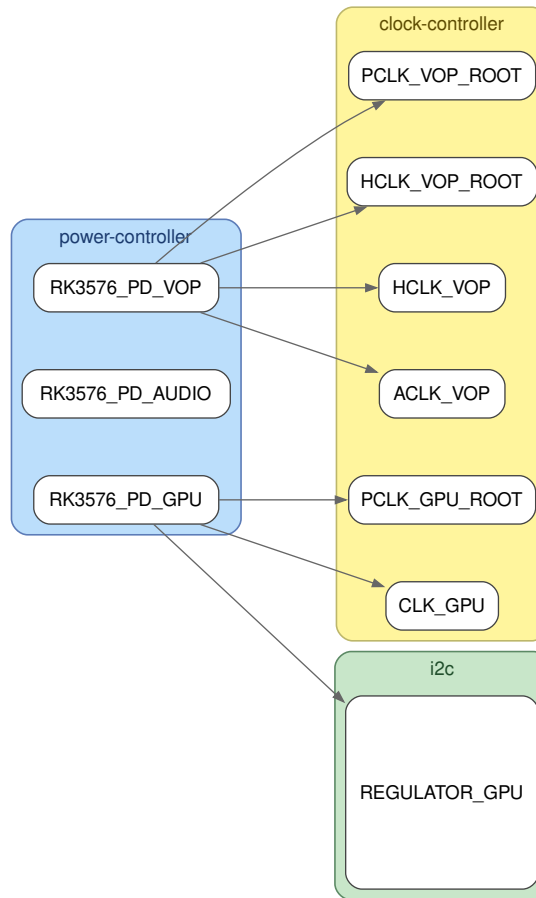
COLLABORA

Hardware Cross-Dependencies Solving the Unsolvable

AngeloGioacchino Del Regno
Sebastian Reichel



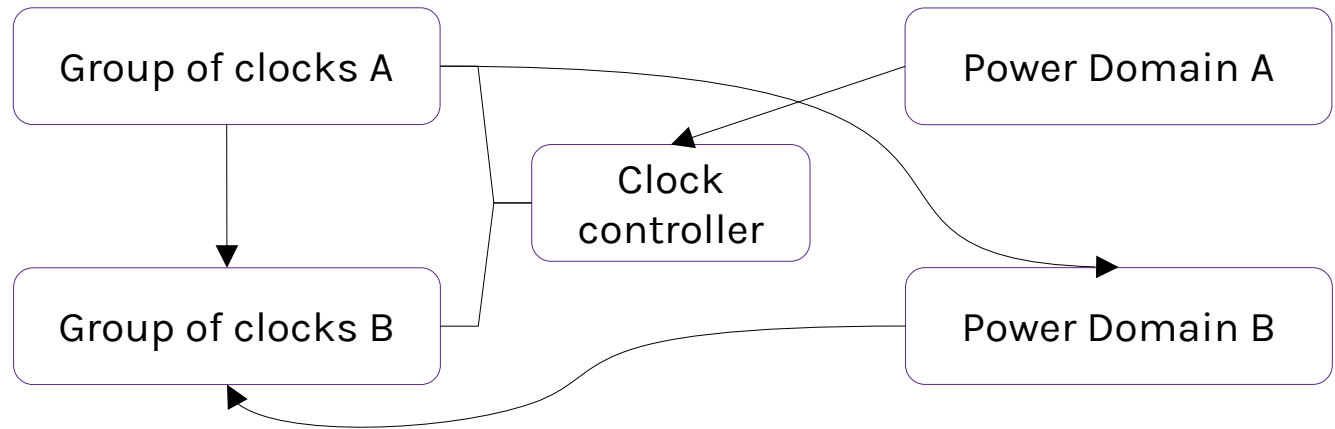
Rockchip power-domain dependencies



Problems

- fw_devlink works on device granularity
 - clocks and power-domains are not devices
- fw_devlink works on fwnode granularity
 - Dependencies might be different based on phandle arguments
 - e.g. <&pmdomains AUDIO> might be ready before <&pmdomain GPU>

MediaTek Power/Clocks dependencies



“Moving the clock controller to the left makes the graph readable”

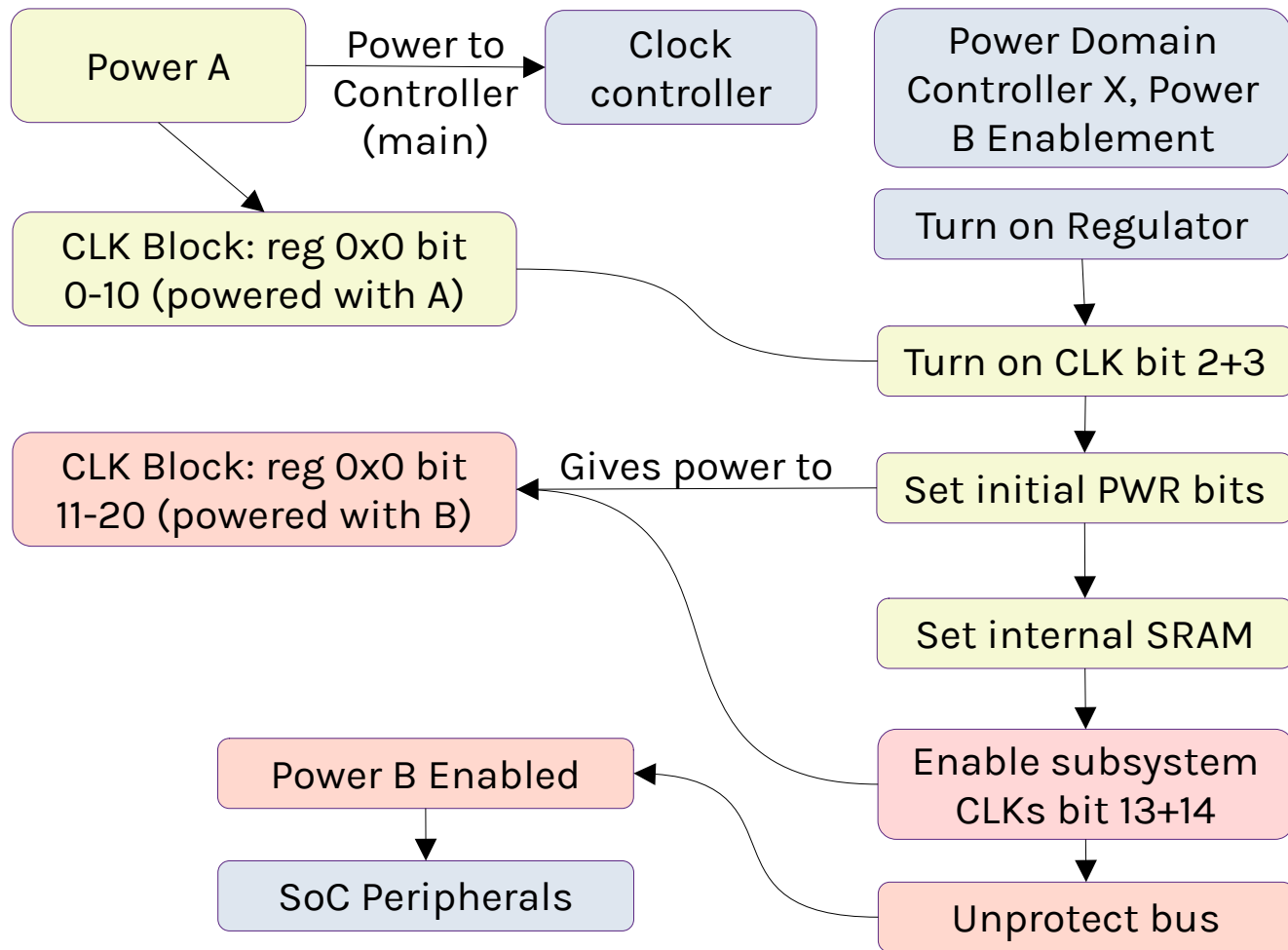
Yes I know, that’s done on purpose.

Just getting your brain ready: the worst is yet to come!

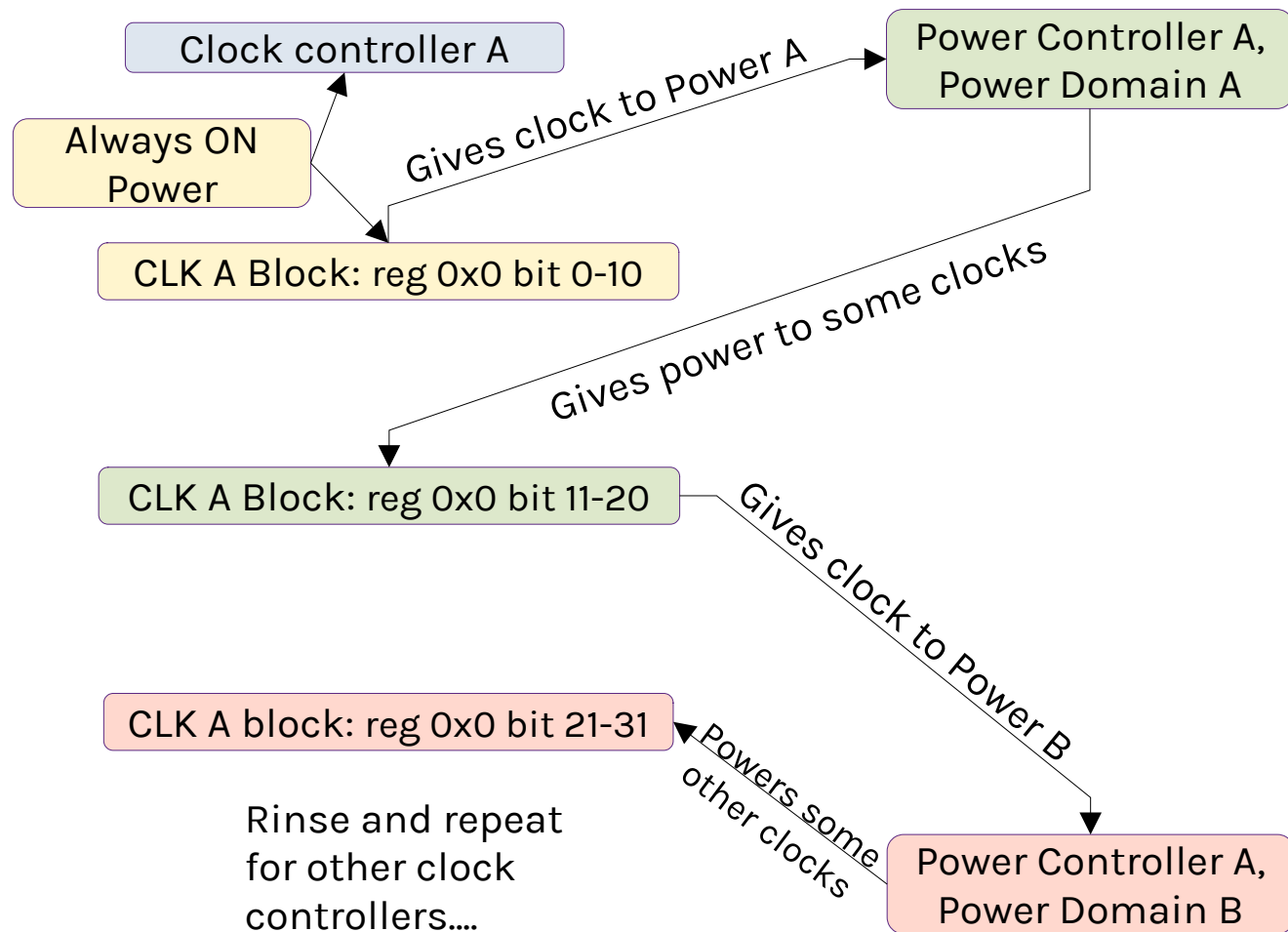
Structure of a MediaTek SoC (in brief)

- Many “full-fledged” macro-blocks
 - Each of those is self-contained
 - Each of those have their own:
 - Power input and, in some cases, output
 - Full Clock Controller
 - Full Reset Controller
 - ...etc
 - Each of those are partially or fully interconnected
 - One or some of them may be required to enable the other

MediaTek Power Controller power-up sequence



MediaTek Clock/Power ...another version



MediaTek Dependencies

- All partial dependencies
 - A single clock controller Y has multiple gate clocks in one register
 - Gate A, B, C: Powered by Power Controller X, Power Domain A
 - For example, Bits 0, 1, 2 in register 0x0
 - Gate D, E, F: Powered by Power Controller X, Power Domain B
 - For example, Bits 3, 4, 5 in register 0x0 (!)
 - A single power domain controller X has multiple domains in one register
 - Power domain A, B, C: Clocked by Clock Controller Y, Gate bits 0, 1
 - Power domain D, E, F: Clocked by Clock Controller Y, Gate bits 4, 5

Note: Reading Gate status needs power to be ON for specific clock bit.



LINUX
PLUMBERS
CONFERENCE

PRAGUE, CZECHIA / OCT. 5-7, 2026



Thank you!



COLLABORA

Open First



LINUX
PLUMBERS
CONFERENCE

PRAGUE, CZECHIA / OCT. 5-7, 2026



We are hiring
col.la/careers



COLLABORA

Open First