

Long-term latency monitoring of real-time Linux systems

Jan Altenberg

Open Source Automation Development Lab (OSADL) eG



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whoami



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About OSADL

REGULAR MEMBERS *GOLD*

A4nXT				
				
				
				

REGULAR MEMBERS *BRONZE*

AS OF AUGUST 2020

OSADL provides everything that is needed to **use, distribute and license FOSS components in industrial products.**

This includes the software itself, but also considers quality, licensing and compliance as well as safety and security aspects.

The OSADL business model is based on the principle:

“Develop once for the use of many.”



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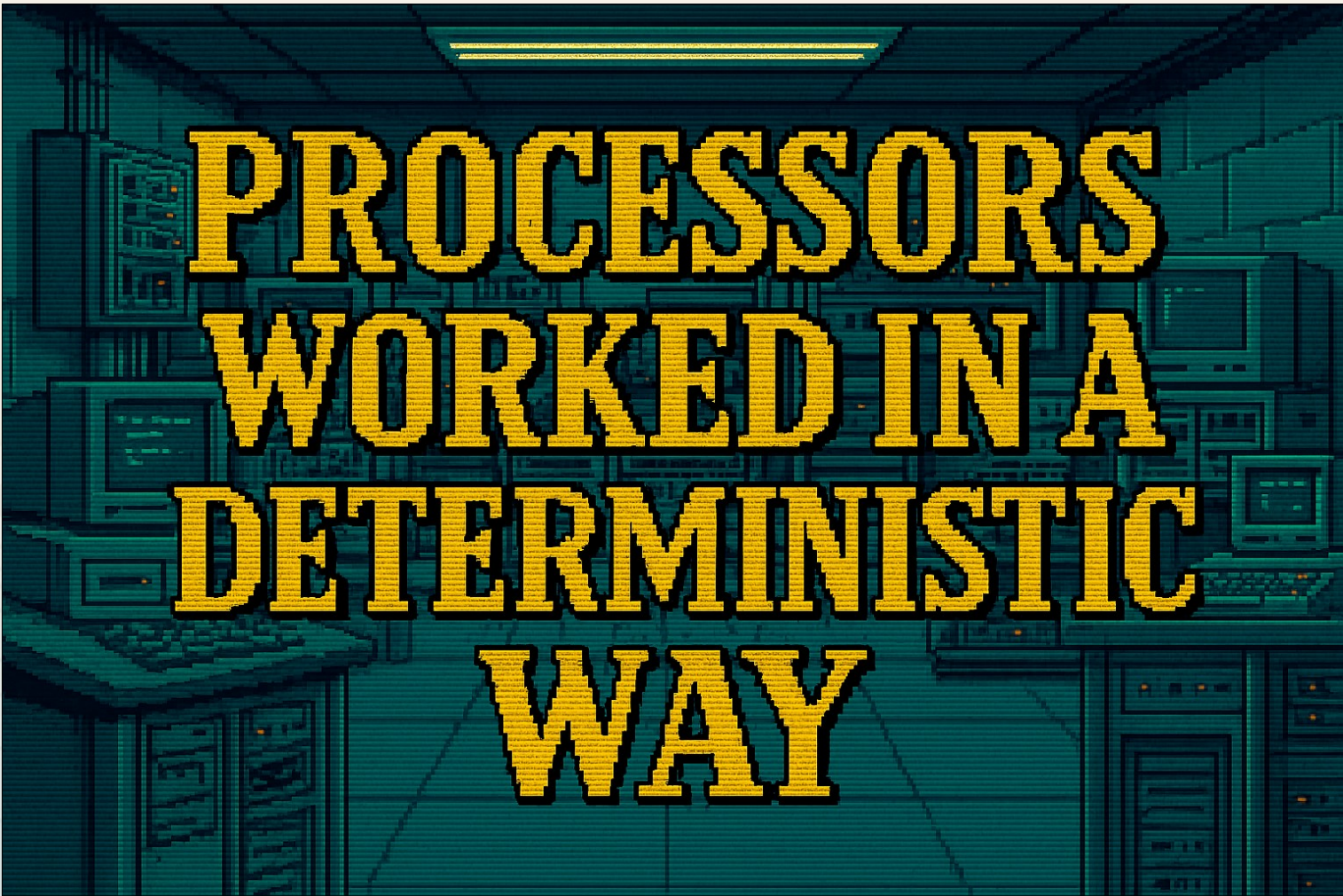
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PROCESSORS WORKED IN A DETERMINISTIC WAY

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1979, Motorola MC68000 @ 8 MHz
(600 Dhrystones)



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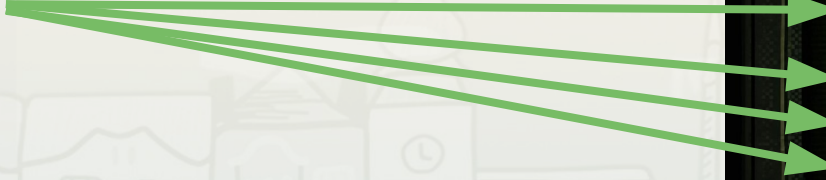
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1979, Motorola MC68000 @ 8 MHz
(600 Dhrystones)

Fetch
instructions from
memory and
execute them.



```
MOVE.L #DRAM,A0  
MOVE.L (A0),D0  
ADD.L #1,D0  
MOVE.L D0,(A0)
```

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(600 Dhrystones)

Fetch
instructions from
memory and
execute them.
Duration = 56
processor cycles



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(600 Dhrystones)

Fetch
instructions from
memory and
execute them.
Duration = 56
processor cycles

SLOW.



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Fetch
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execute them.
Duration = 56
processor cycles



```
MOVE.L #DRAM,A0  
MOVE.L (A0),D0  
ADD.L #1,D0  
MOVE.L D0,(A0)
```

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**SLOW,
BUT DETERMINISTIC**



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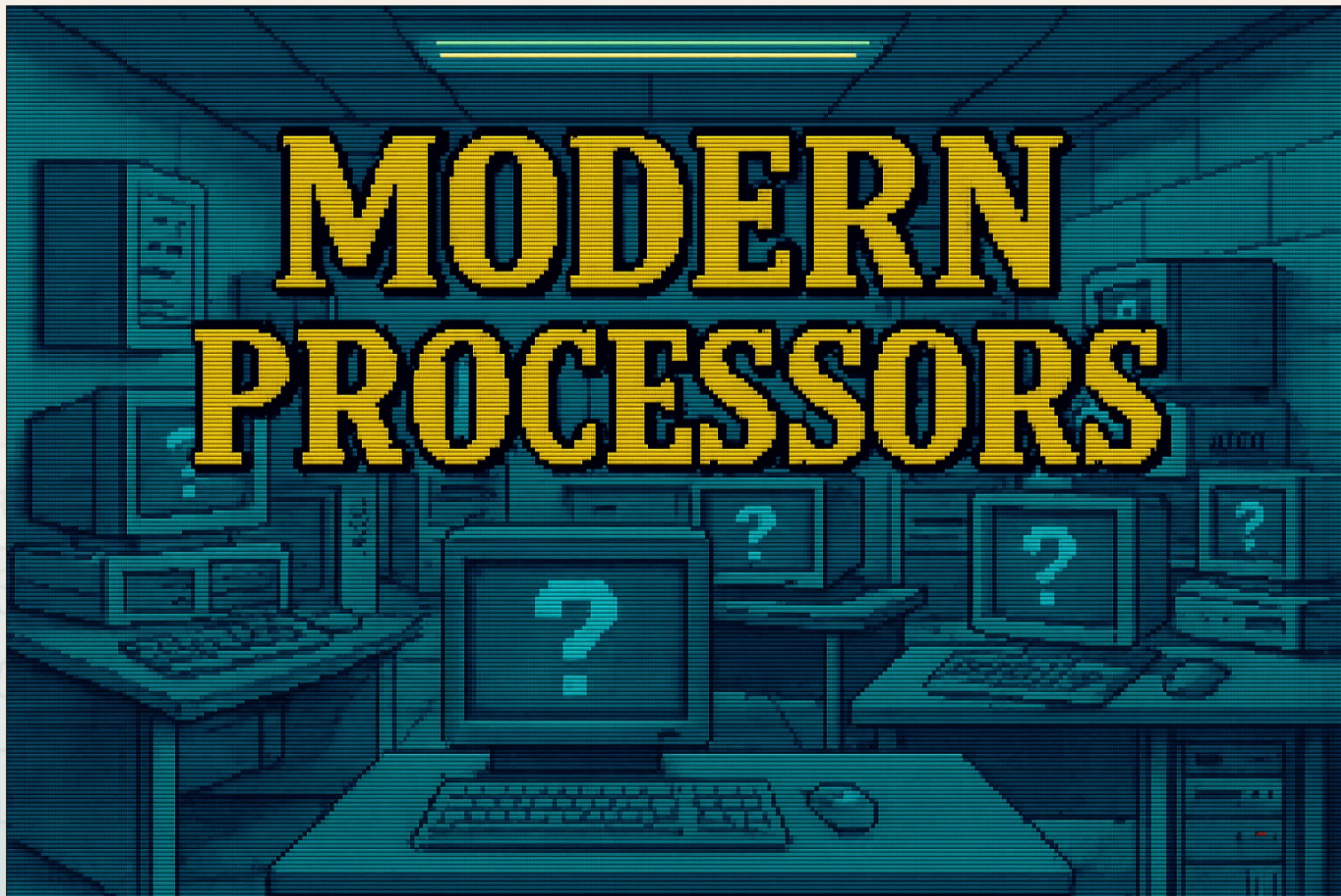
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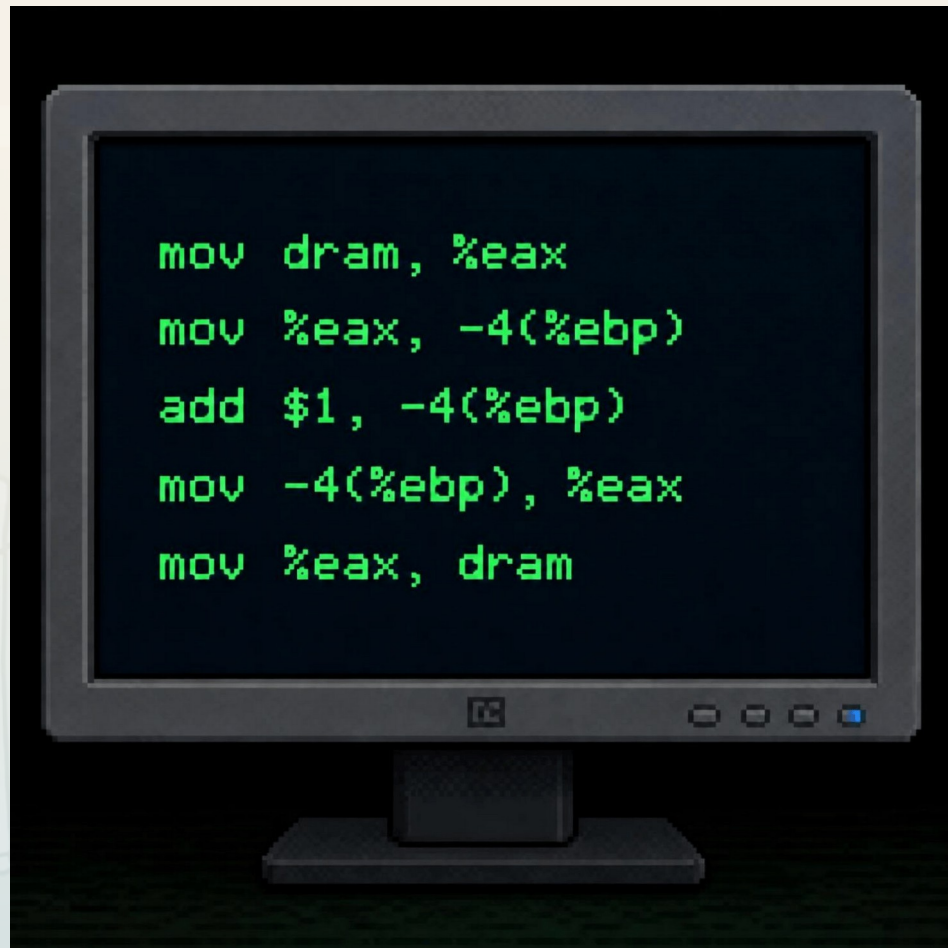
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2009, x86 processor @ 3 GHz
(12.000.000 Dhrystones)

Fetch
instructions from
memory and
execute them.

```
mov dram, %eax  
mov %eax, -4(%ebp)  
add $1, -4(%ebp)  
mov -4(%ebp), %eax  
mov %eax, dram
```

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2009, x86 processor @ 3 GHz
(12.000.000 Dhrystones)

Fetch
instructions from
memory and
execute them.
Duration = ?????
processor cycles



```
mov dram, %eax  
mov %eax, -4(%ebp)  
add $1, -4(%ebp)  
mov -4(%ebp), %eax  
mov %eax, dram
```

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Instruction not in cache



2009, x86 processor @ 3 GHz
(12.000.000 Dhrystones)

```
mov dram, %eax
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mov -4(%ebp), %eax
mov %eax, dram
```

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Instruction not in cache



**Data not in cache/no free
cache lines**



2009, x86 processor @ 3 GHz
(12.000.000 Dhrystones)



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Instruction not in cache



**Data not in cache/no free
cache lines**



**System Management
Interrupt**



2009, x86 processor @ 3 GHz
(12.000.000 Dhrystones)



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Instruction not in cache



**Data not in cache/no free
cache lines**



**System Management
Interrupt**



**Instruction may need to be
emulated (microcode patch)**



2009, x86 processor @ 3 GHz
(12.000.000 Dhrystones)



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Instruction not in cache



**Data not in cache/no free
cache lines**



**System Management
Interrupt**



**Instruction may need to be
emulated (microcode patch)**



2009, x86 processor @ 3 GHz
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FAST, BUT RANDOM

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Challenge

- Transition:
 - from static code analysis to dynamic system analysis
 - from theoretical approach to empirical testing
 - from transition from one paradigm to another



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Evaluation methods

- External measurement with simulation (e.g. function generator)
- Internal latency registration (e.g. RTLA, OSADL patches)
- Internal measurement with simulation (e.g. cyclicttest)



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OSADL QA Farm



<https://www.osadl.org/QA>



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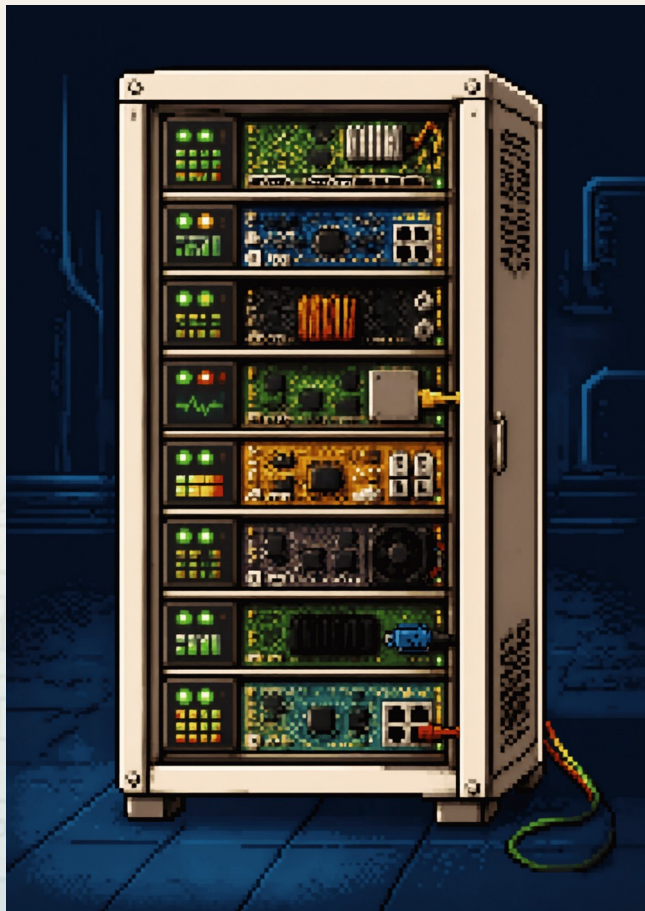
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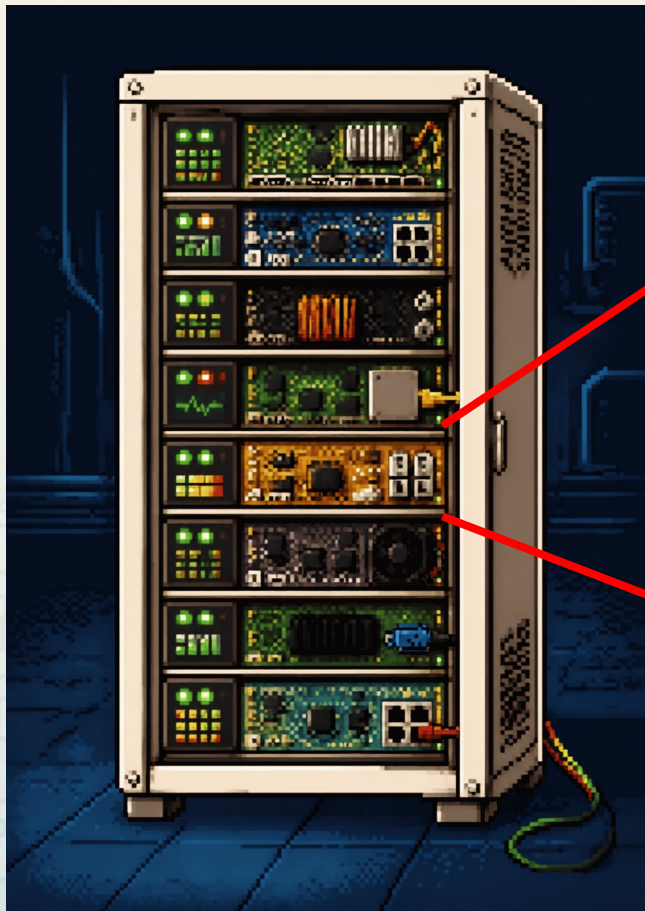
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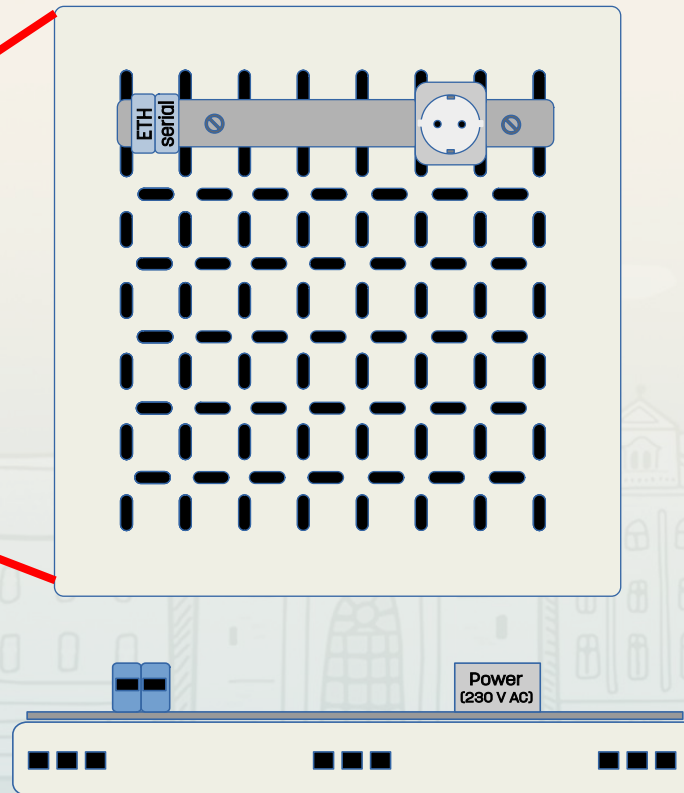


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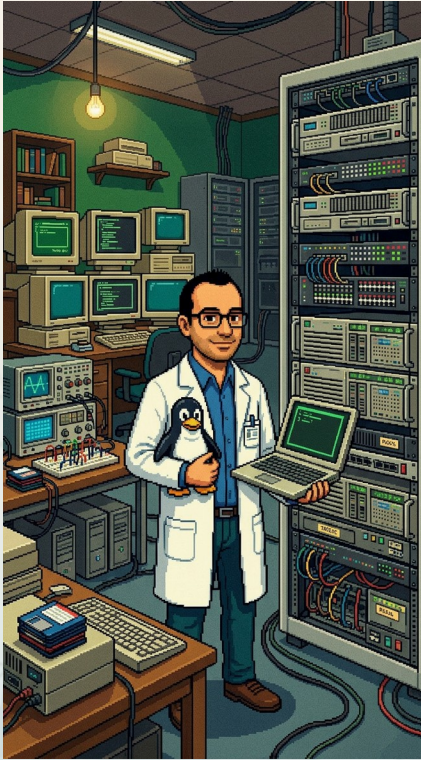


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Data being recorded



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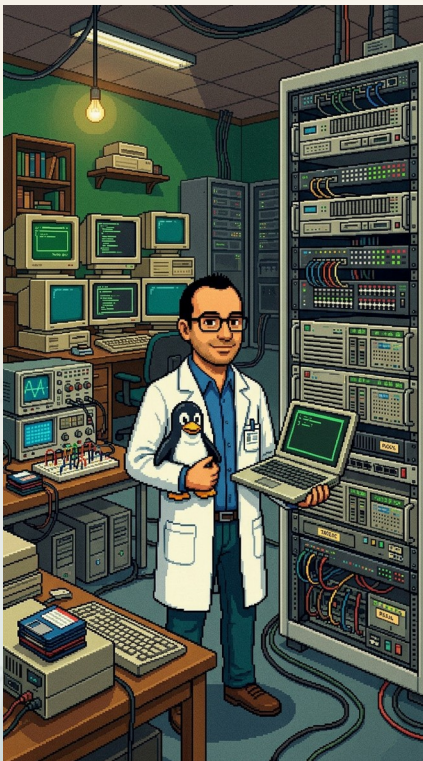
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Data being recorded

- Static data (vendor / board, kernel version, kernel configuration, ...)



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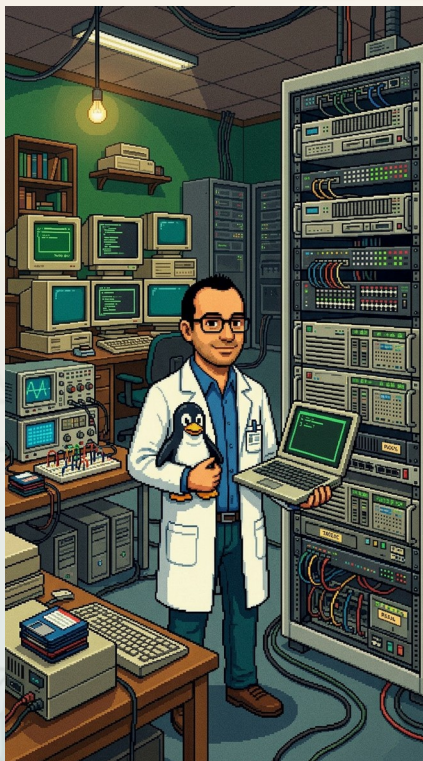
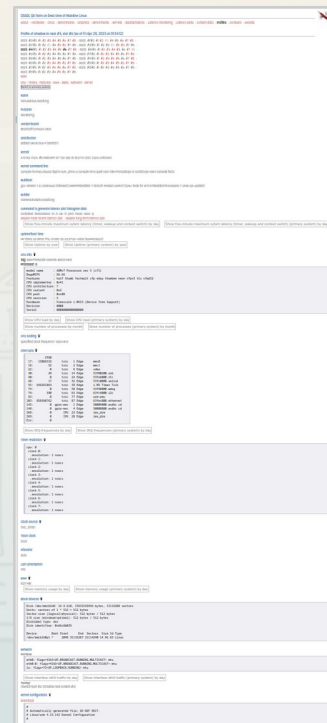
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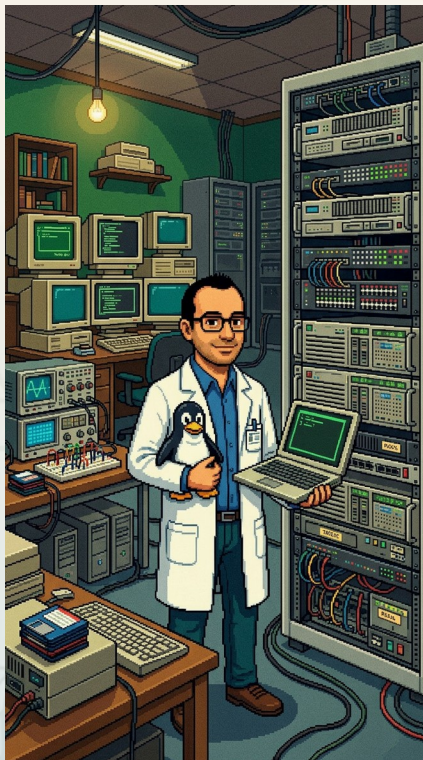
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Data being recorded

- Static data (vendor / board, kernel version, kernel configuration, ...)
- Continuous measurements (CPU load, memory consumption, temperatures, uptime, ...)



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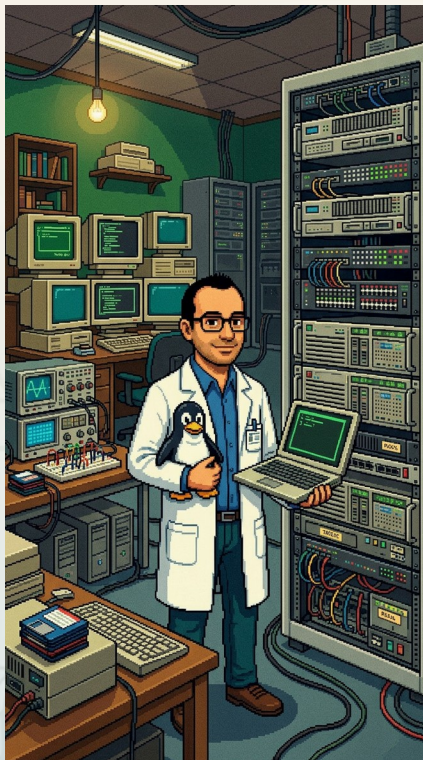
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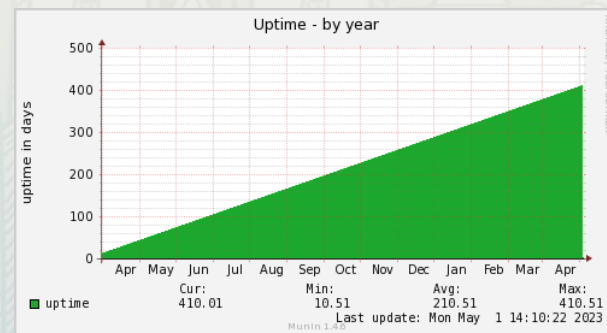
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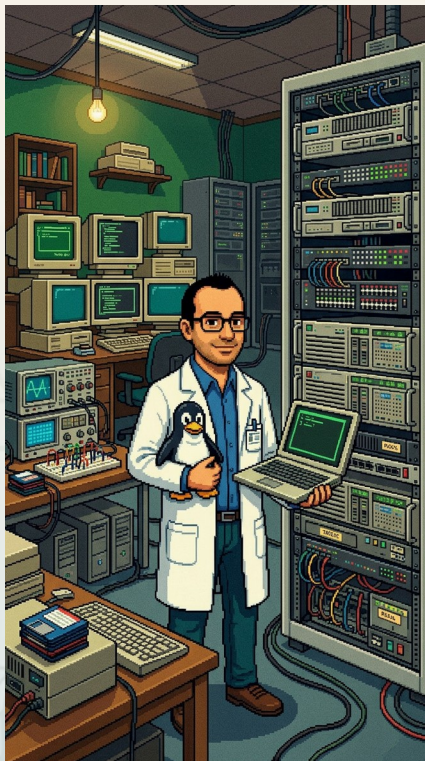
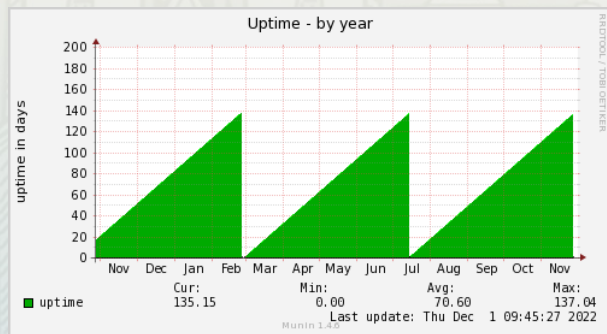
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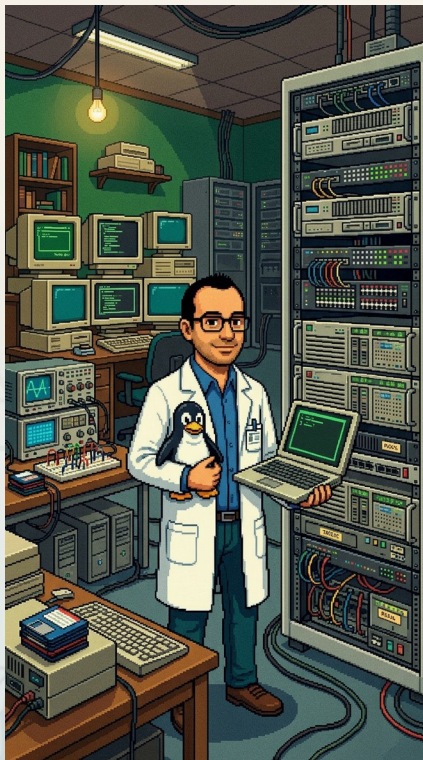
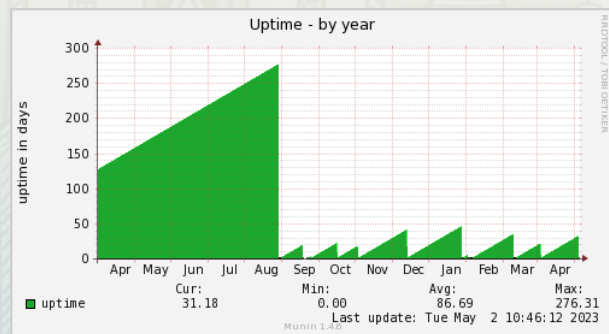
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Data being recorded

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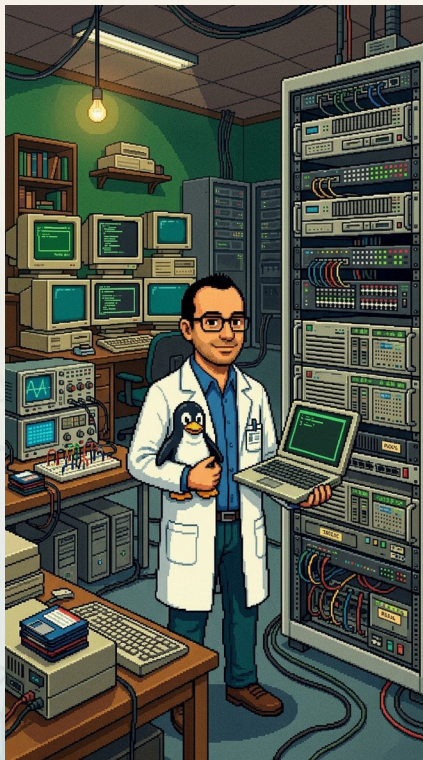
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Data being recorded



- Static data (vendor / board, kernel version, kernel configuration, ...)
- Continuous measurements (CPU load, memory consumption, temperatures, uptime, ...)
- Latency measurements

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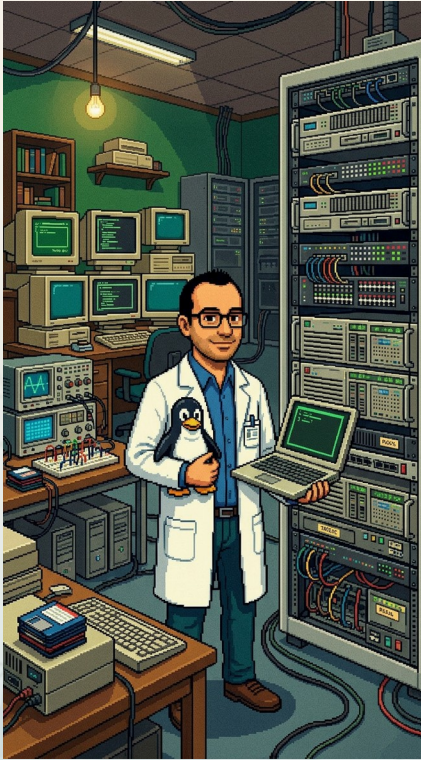
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Data being recorded



- Static data (vendor / board, kernel version, kernel configuration, ...)
- Continuous measurements (CPU load, memory consumption, temperatures, uptime, ...)
- **Latency measurements**

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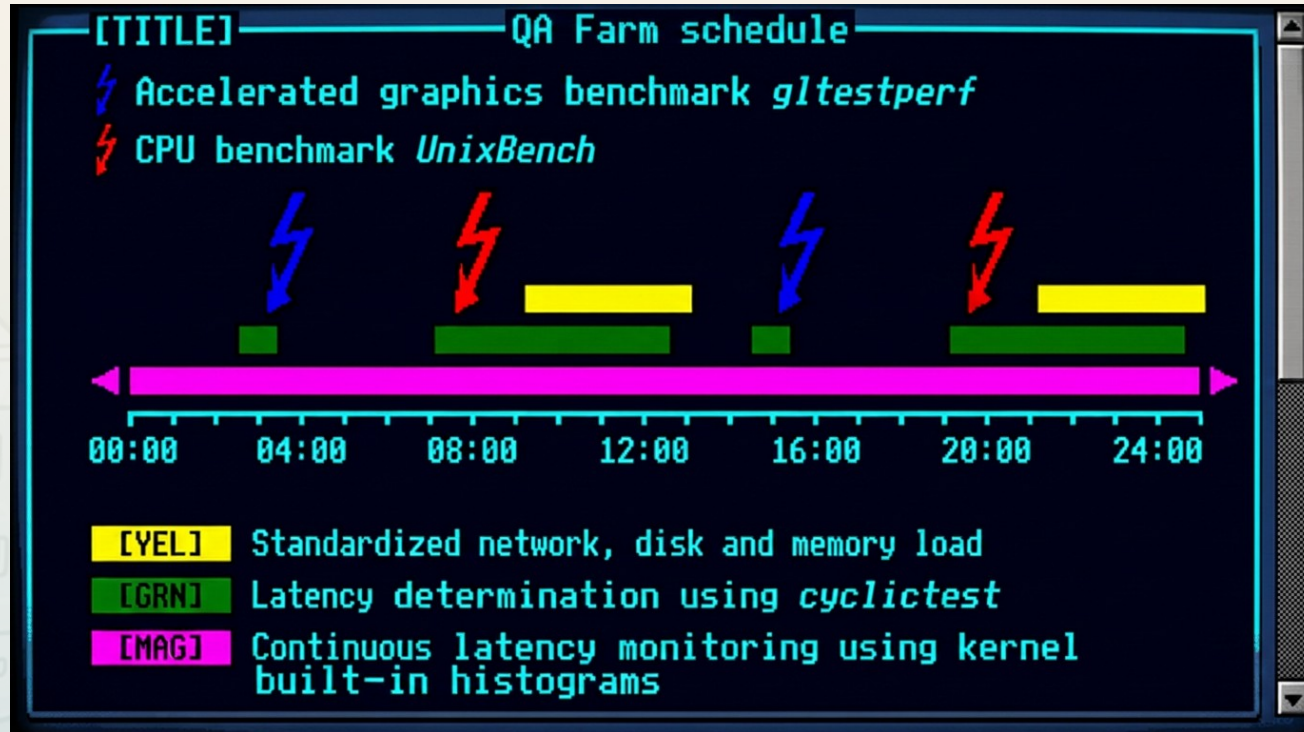
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QA Farm schedule



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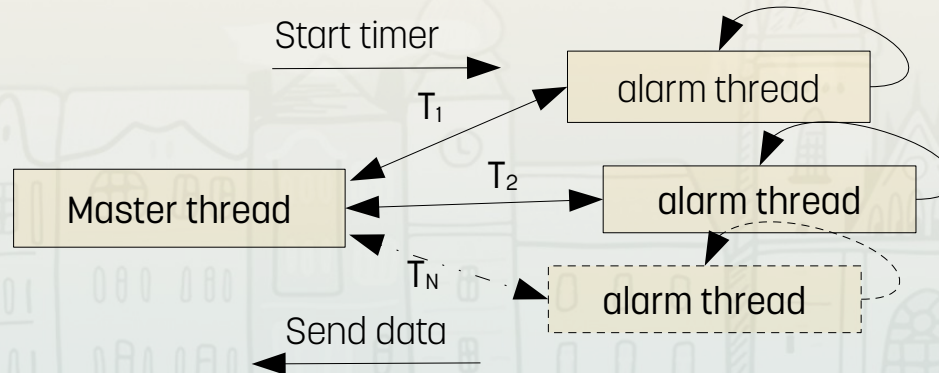
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Validation of real-time processing: cyclicttest

Determination by a **simulated real-time application** (cyclicttest):



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Latency measurement

Run one thread per CPU Priority 98
Interval 200us
Run all threads at the same interval

Lock memory

```
# cyclicttest -m -S -i200 -p98 -D0
```

T: 0 (26623) P:98 I:200 C:2244063 Min: 2 Act: 5 Avg: 4 Max: 27

Process ID Cycles Worst-case latency in us



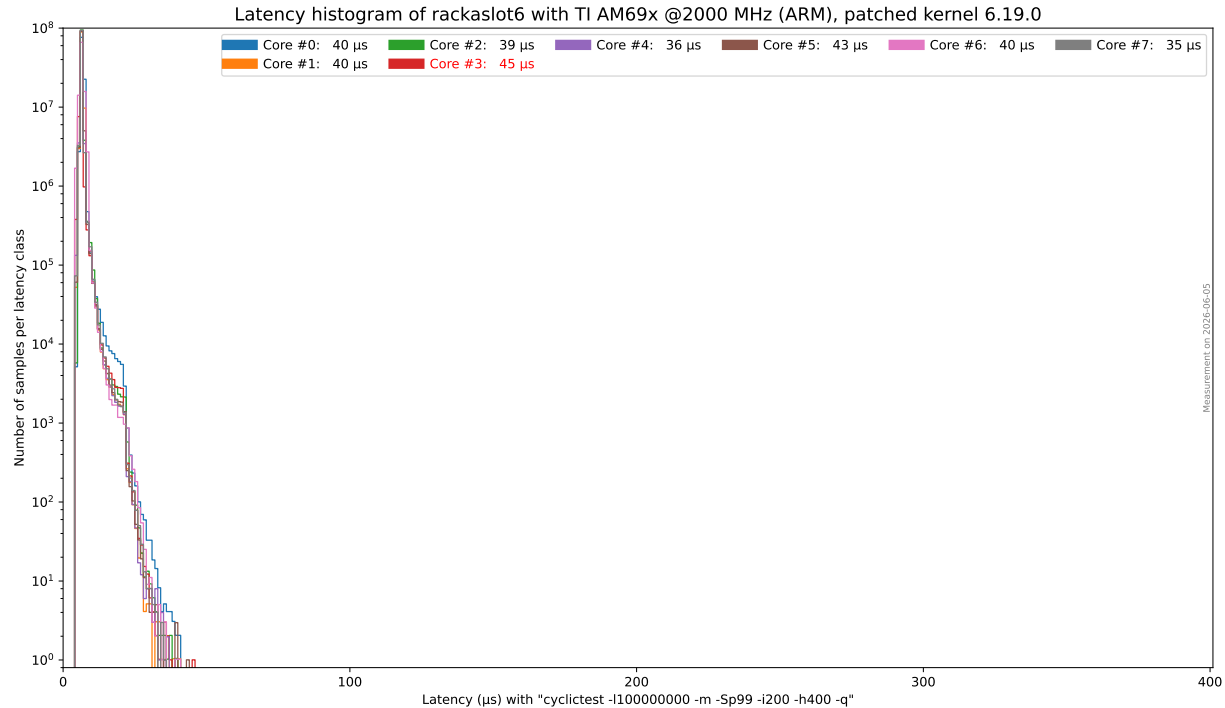
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Example: Latencyplot



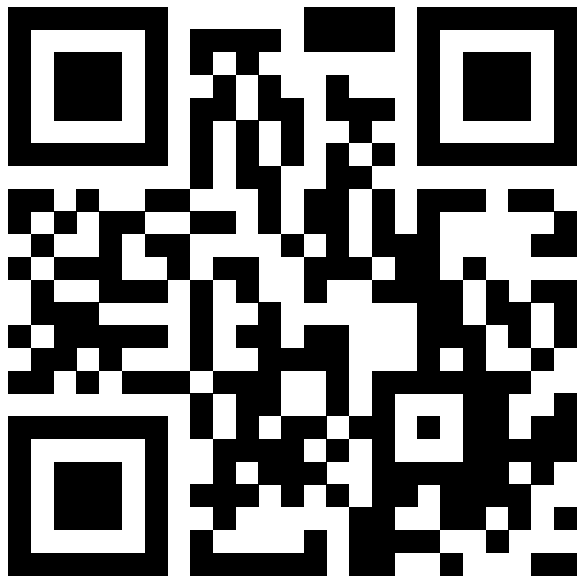
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Latency histograms patch



<https://www.osadl.org/?id=2945>



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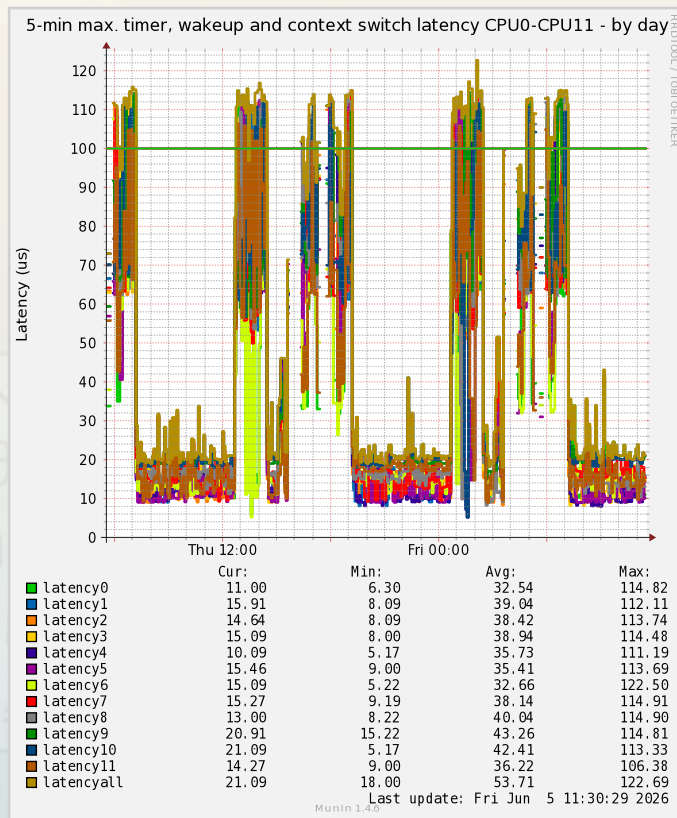


Latency histograms



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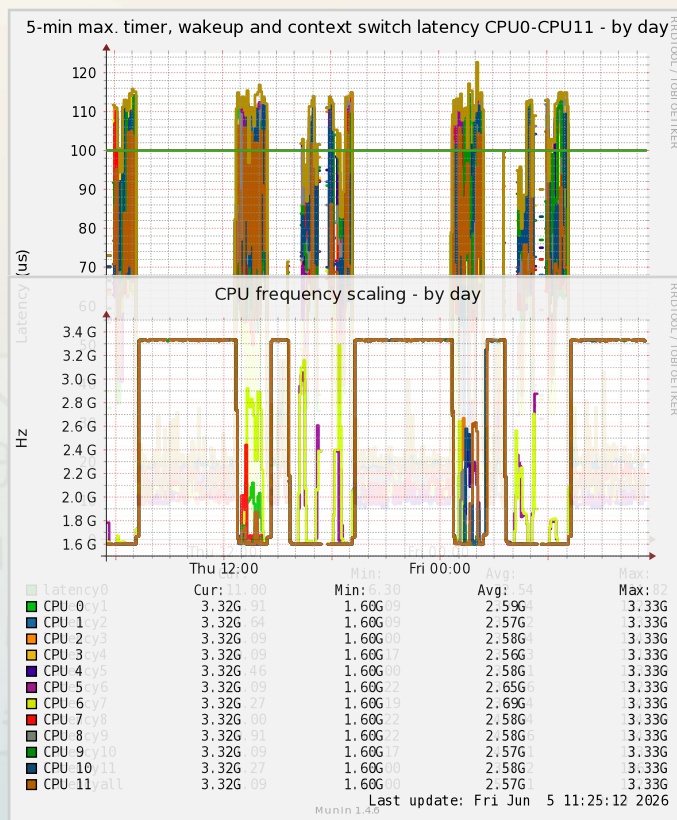
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Latency histograms



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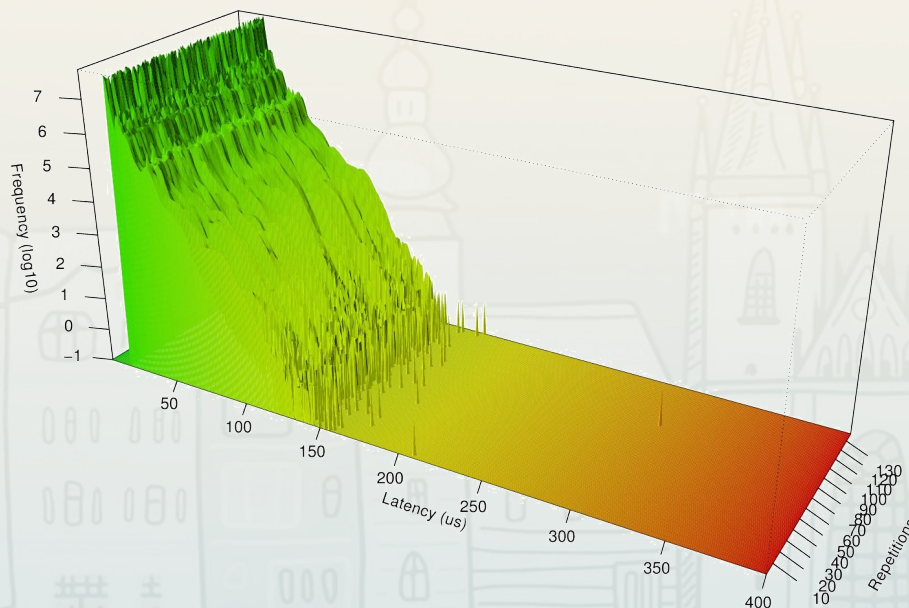
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Long-term latency plots

System in rack #b, slot #7
Recording from 02.01.2026 until 14.03.2026



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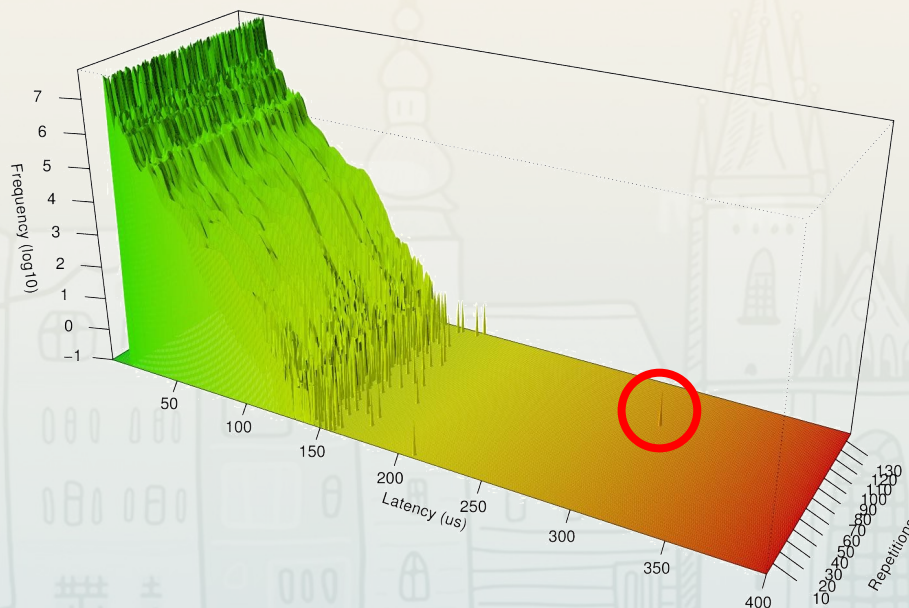
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Long-term latency plots

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Latency histograms

```
# cyclicttest -m -S -i200 -d0 -p99
```

```
# /dev/cpu_dma_latency set to 0us
```

```
policy: fifo: loadavg: 0.05 0.06 0.02 1/131 493
```

T: 0 (474)	P:99	I:200	C: 81314	Min: 6	Act: 9	Avg: 8	Max: 4952
T: 1 (475)	P:99	I:200	C: 81243	Min: 6	Act: 9	Avg: 8	Max: 4987
T: 2 (476)	P:99	I:200	C: 81191	Min: 6	Act: 9	Avg: 8	Max: 4880
T: 3 (477)	P:99	I:200	C: 81124	Min: 6	Act: 11	Avg: 8	Max: 4886



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Latency histograms

```
# cd /sys/kernel/debug/latency_hist/timerandwakeup
```

```
# cat max_latency-CPU*
```

```
546 99 4988 (4964,0) cyclicttest <- 552 -21 mklatency 440.676730
```

```
547 99 4875 (4849,0) cyclicttest <- 553 -21 mklatency 440.687647
```

```
548 99 4929 (4909,0) cyclicttest <- 554 -21 mklatency 440.697379
```

```
549 99 4874 (4849,0) cyclicttest <- 555 -21 mklatency 440.707655
```



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Latency histograms

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548 99 4929 (4909,0) cyclicttest <- 554 -21 mklatency 440.697379
549 99 4874 (4849,0) cyclicttest <- 555 -21 mklatency 440.707655
```

Victim



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Latency histograms

```
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```
# cat max_latency-CPU*
```

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546 99 4988 (4964,0) cyclicttest <- 552 -21 mklatency 440.676730
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549 99 4874 (4849,0) cyclicttest <- 555 -21 mklatency 440.707655
```

Priority



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Latency histograms

```
# cd /sys/kernel/debug/latency_hist/timerandwakeup
```

```
# cat max_latency-CPU*
```

```
546 99 4988 (4964,0) cyclicttest <- 552 -21 mklatency 440.676730
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549 99 4874 (4849,0) cyclicttest <- 555 -21 mklatency 440.707655
```

**Latency
(us)**



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Long-term latency monitoring of real-time Linux systems
Open Source Automation Development Lab (OSADL), Heidelberg



Latency histograms

```
# cd /sys/kernel/debug/latency_hist/timerandwakeup
```

```
# cat max_latency-CPU*
```

546	99	4988	(4964,0)	cyclictest	<-	552	-21	mklatency	440.676730
547	99	4875	(4849,0)	cyclictest	<-	553	-21	mklatency	440.687647
548	99	4929	(4909,0)	cyclictest	<-	554	-21	mklatency	440.697379
549	99	4874	(4849,0)	cyclictest	<-	555	-21	mklatency	440.707655

Culprit



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Latency histograms

```
# cd /sys/kernel/debug/latency_hist/timerandwakeup
```

```
# cat max_latency-CPU*
```

```
546 99 4988 (4964,0) cyclicttest <- 552 -21 mklatency 440.676730
547 99 4875 (4849,0) cyclicttest <- 553 -21 mklatency 440.687647
548 99 4929 (4909,0) cyclicttest <- 554 -21 mklatency 440.697379
549 99 4874 (4849,0) cyclicttest <- 555 -21 mklatency 440.707655
```

Priority



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Latency histograms

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546 99 4988 (4964,0) cyclictst <- 552 -21 mklatency 440.676730
547 99 4875 (4849,0) cyclictst <- 553 -21 mklatency 440.687647
548 99 4929 (4909,0) cyclictst <- 554 -21 mklatency 440.697379
549 99 4874 (4849,0) cyclictst <- 555 -21 mklatency 440.707655
```

Timestamp



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Latency histograms

Delayed (victim)					Switcher (culprit)			Timestamp	CPU
PID	Prio	Total latency (µs)	$T^*(W^{**})$ latency (µs)	Cmd	PID	Prio	Cmd		
2089381	99	171	152,14	cyclicttest	79	-21	hwrng	11:05:33	1



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Back to: Long-term latency plots



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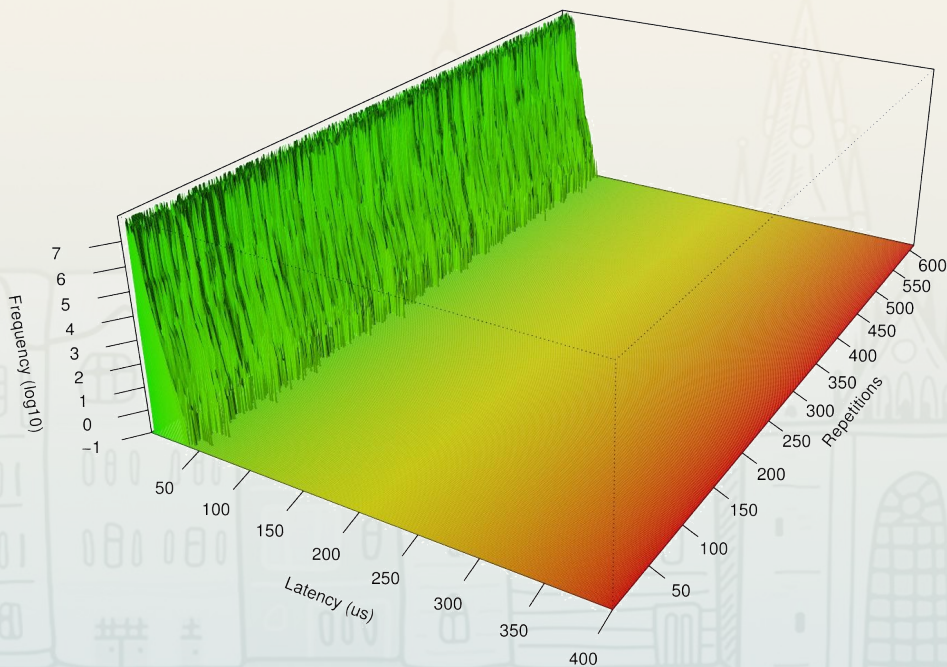
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Long-term latency plots

System in rack #8, slot #3
Recording from 01.01.2020 until 26.12.2020



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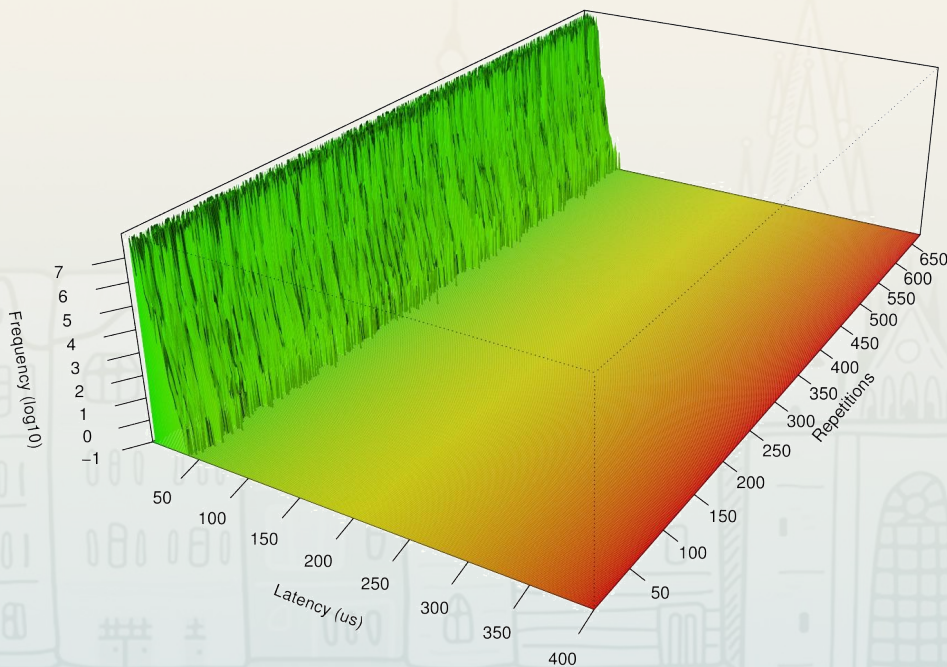
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Long-term latency plots

System in rack #8, slot #3
Recording from 01.01.2021 until 25.12.2021



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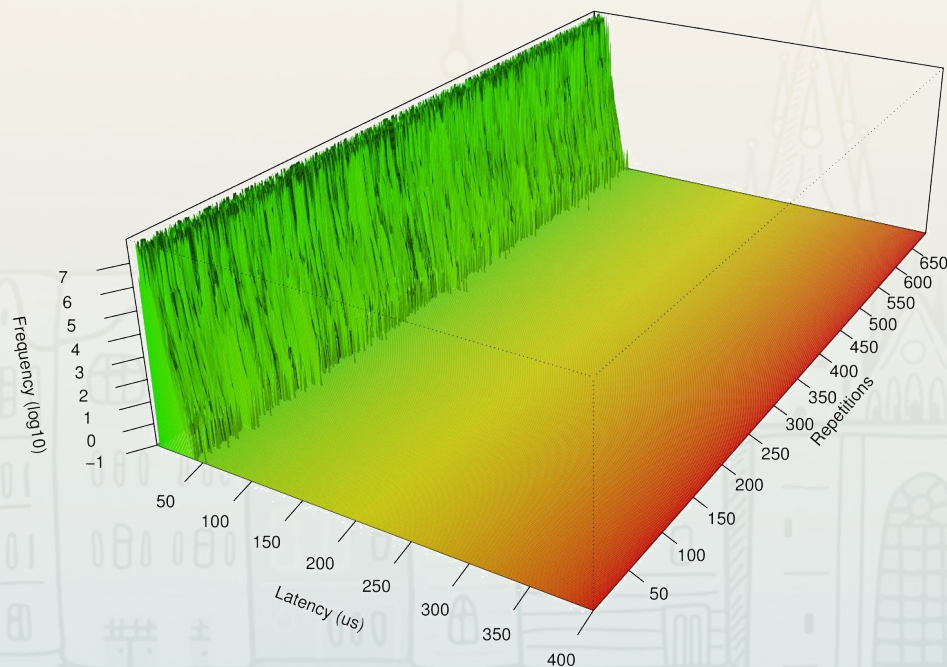
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Long-term latency monitoring of real-time Linux systems
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Long-term latency plots

System in rack #8, slot #3
Recording from 01.01.2022 until 31.12.2022



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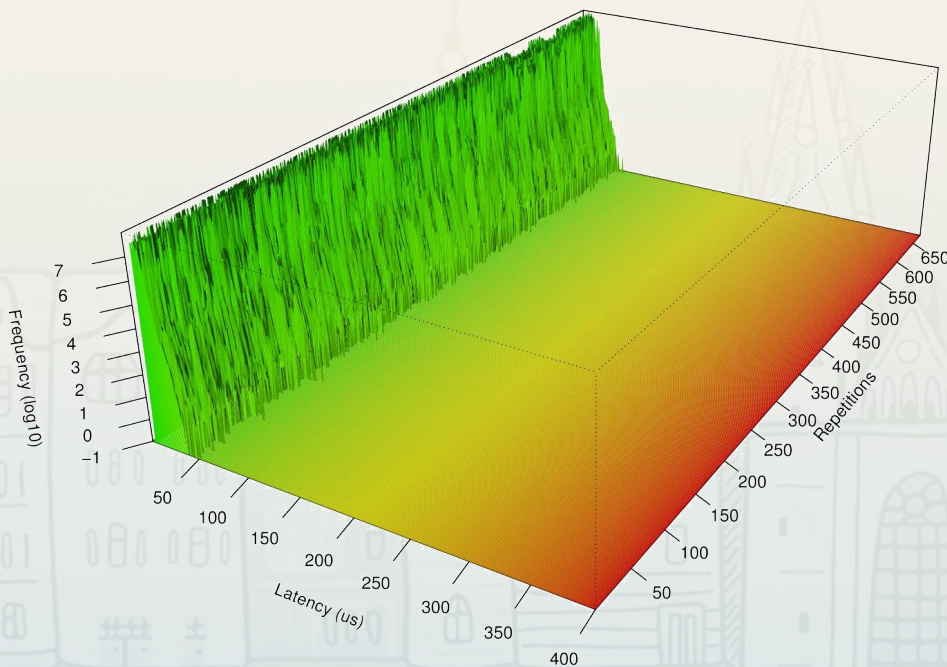
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Long-term latency monitoring of real-time Linux systems
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Long-term latency plots

System in rack #8, slot #3
Recording from 01.01.2023 until 30.12.2023



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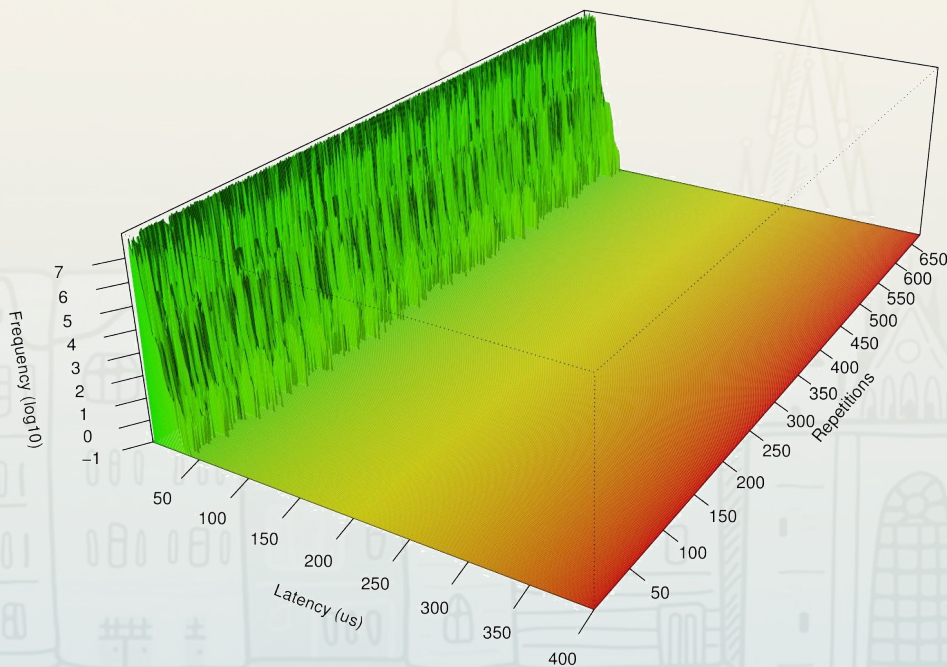
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System in rack #8, slot #3
Recording from 01.01.2024 until 28.12.2024



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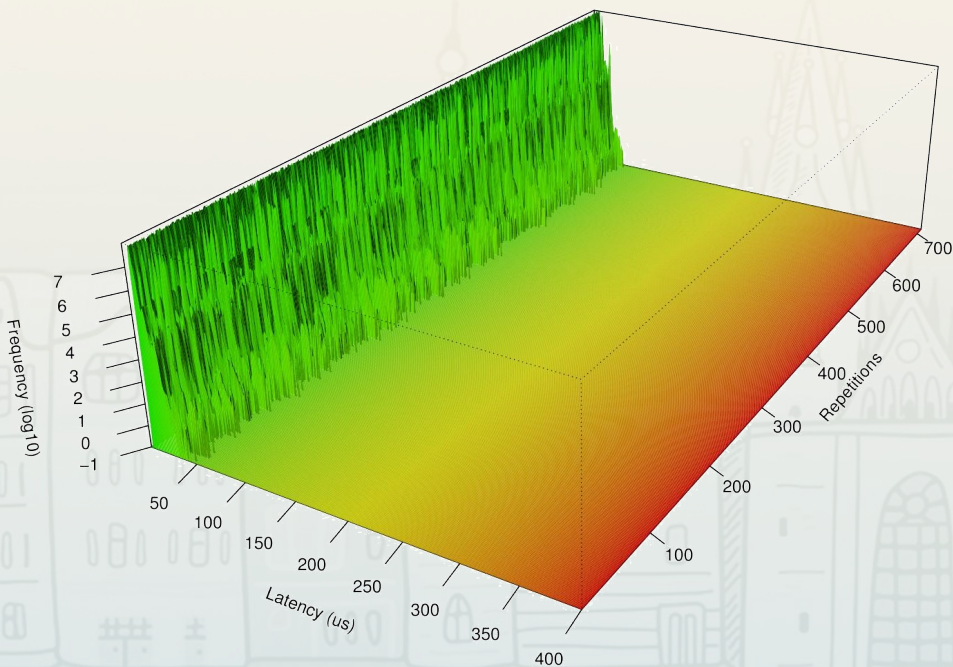
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Long-term latency plots

System in rack #8, slot #3
Recording from 01.01.2025 until 27.12.2025



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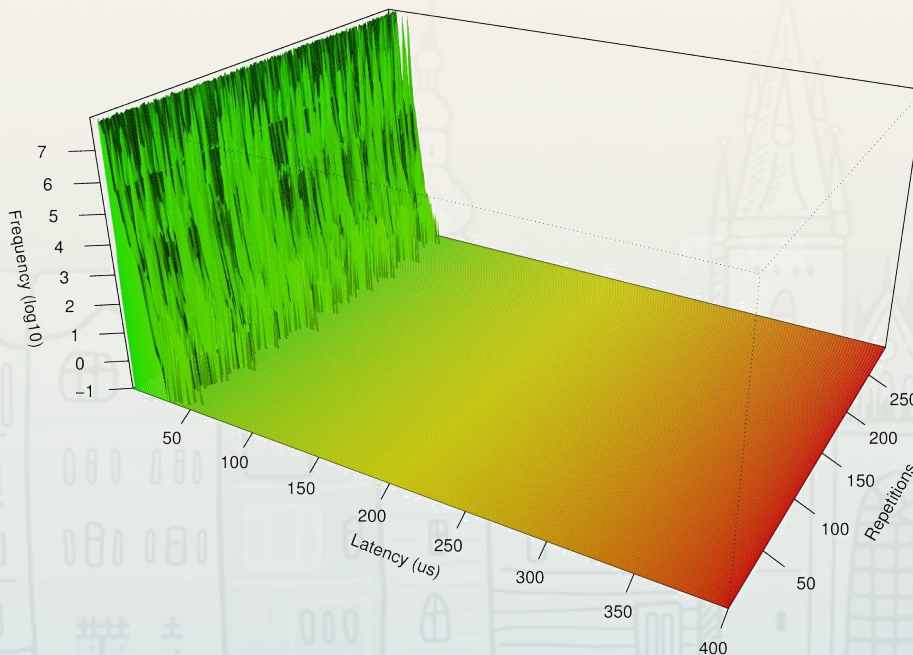
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Long-term latency plots

System in rack #8, slot #3
Recording from 01.01.2026 until 30.05.2026



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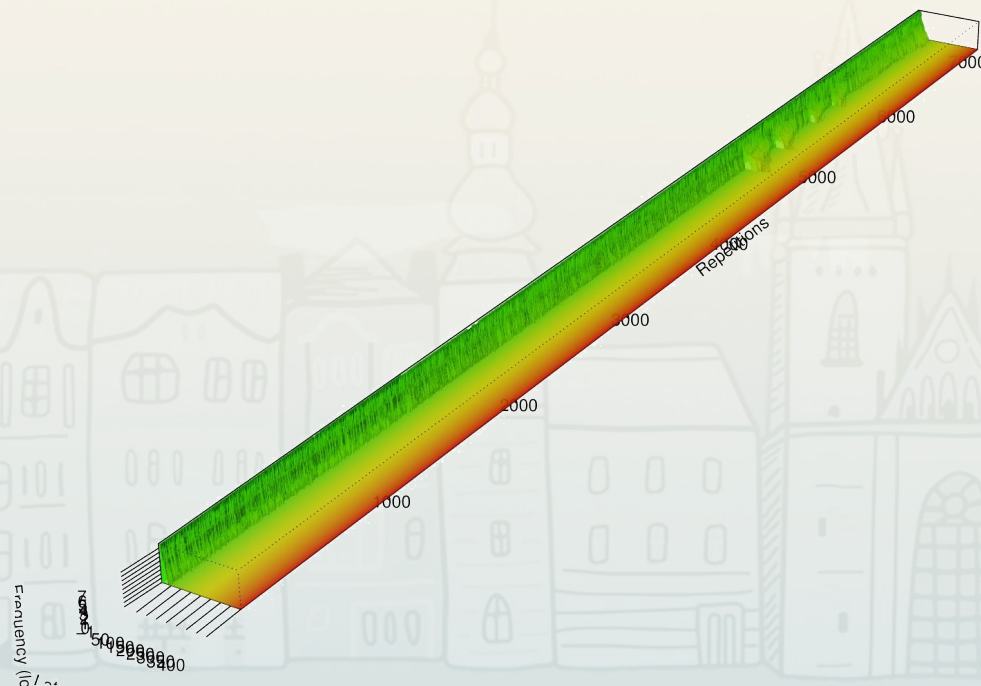
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Long-term latency plots

System in rack #8, slot #3
Recording from 01.01.2016 until 01.06.2026



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Future work / Topics for discussion

- Context information in latency plots
- Load generation scenarios / stress-ng
- RTLA



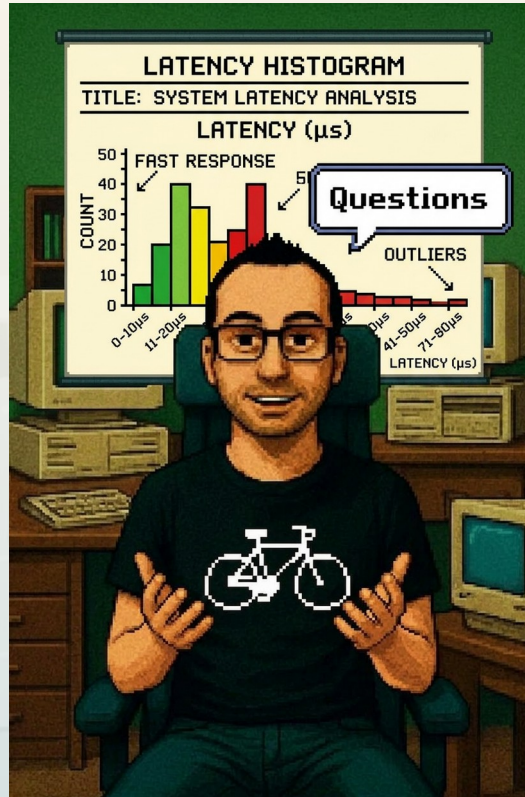
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Questions?



AI generated content (Canva Business)



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