



Contribution ID: 240

Type: **not specified**

Supervisor Binary Interface(SBI) extension in RISC-V

Thursday, November 15, 2018 9:30 AM (30 minutes)

This is a proposal to make SBI a flexible and extensible interface. It is based on the foundation policy of RISC-V i.e. modularity and openness. The current RISC-V SBI only defines a few mandatory functions such as inter-processor interrupts (IPI) interface, reprogramming timer, serial console, and memory barrier instructions. Many important functionalities such as power management/cpu-hotplug are not yet defined due to difficulties in accommodating modifications without breaking the backward compatibility with the current interface.

Presenter: PATRA, Atish (Western Digital)

Session Classification: RISC-V MC