Contribution ID: **351** Type: **not specified**

Declaring WARL on the ISA string.

A RISC-V ISA has a lot of variables, and the ISA string describes a small subset of those variables, so some of the remaining ones are current discovered by directly interacting with the ISA implementation through trial and error (WARL).

WARL hinders virtualization as the discovery is done through registers that we don't want to trap and emulate for performance reasons, and there is no architectural control over the WARL behavior otherwise, essentially throwing the point of hardware accelerated virtualization out of the window.

It is a bit late to get rid of WARL behavior in the ISA, and there wasn't any interest in adding ISA control over the behavior…

I think the best we can do is to tactfully ignore that WARL exists, and only write known legal values, but that requires a more complete ISA description.
The Unified Database project should eventually describe the whole ISA, so we could be deriving a new DT structure for the ISA from its YAML.

I'd like to have a discussion about the desired DT format, and the direction in general, as we can also choose to discover the ISA through SBI (cpuid style) or even more outlandish methods.

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Session Classification: RISC-V MC

Track Classification: RISC-V MC