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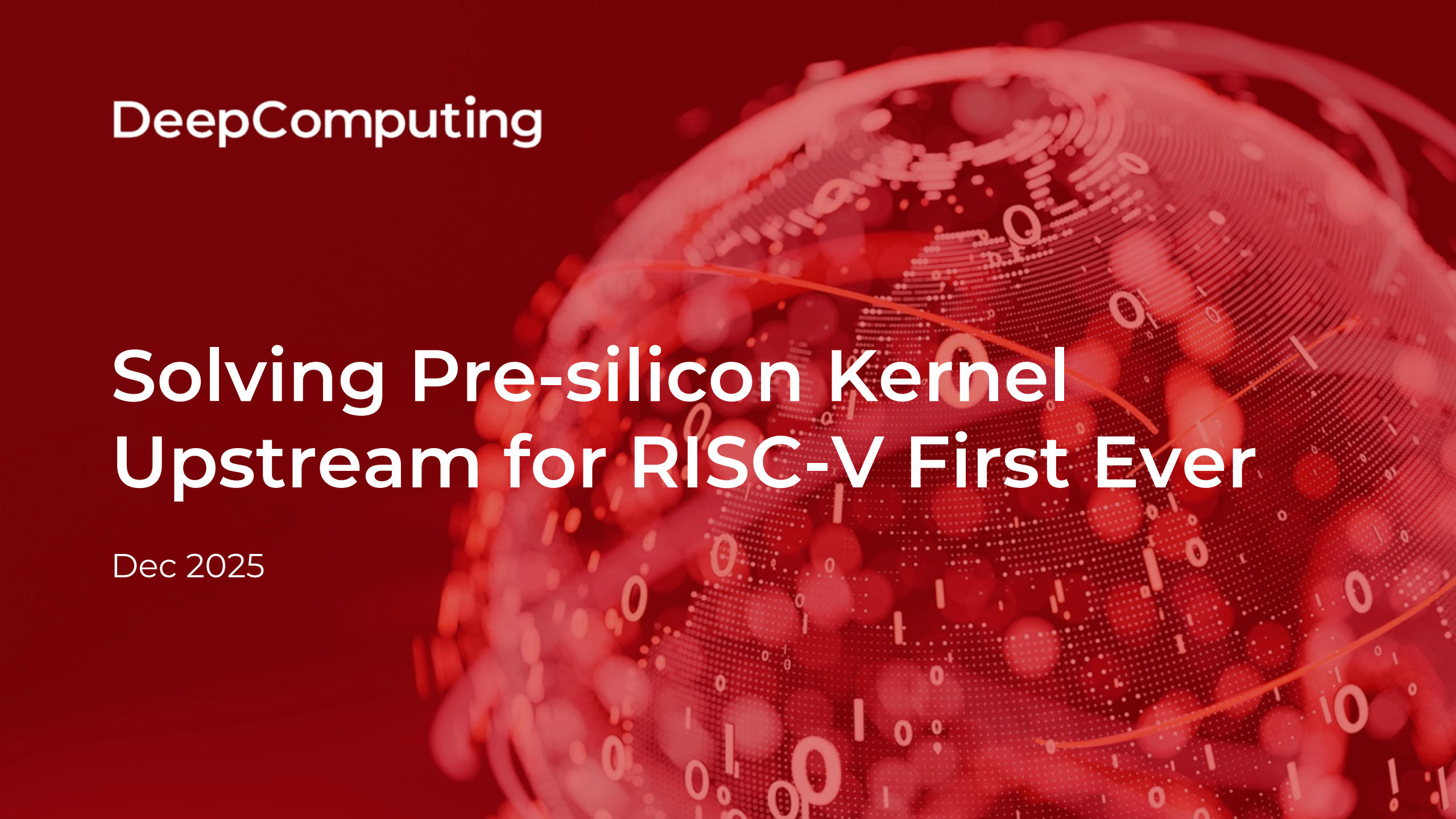
Solving Pre-silicon Kernel Upstream for RISC-V First Ever

Dec 2025



Agenda

- Introduction
- Why Upstreaming?
- How to Achieve Pre-silicon Upstreaming?
- What to Improve!

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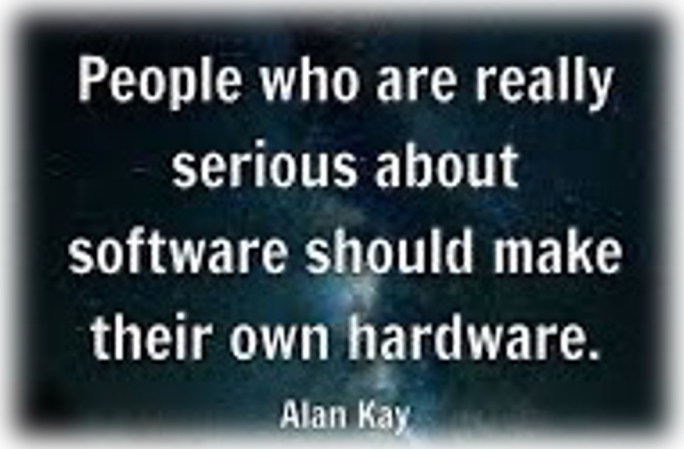
Yuning Liang

Founder

a core software guy

Java VM (J2ME) / Static Compiler (MIPS’ Open64)



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Who are we and What we do

RISC-V Premium Product Pioneer Focusing on

- Consumer Electronics
- Modern Personal Computing Devices
- And Some RISC-V Run & Fun Gadgets






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DC-ROMA RISC-V Laptops/Pad

2023

4-core 1.5GHz

8GDDR

2024

8-core 1.75GHz

16G DDR

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Framework RISC-V AI-PC Product Portfolio

Desktop and
Laptop 12”/13”/14”/16”

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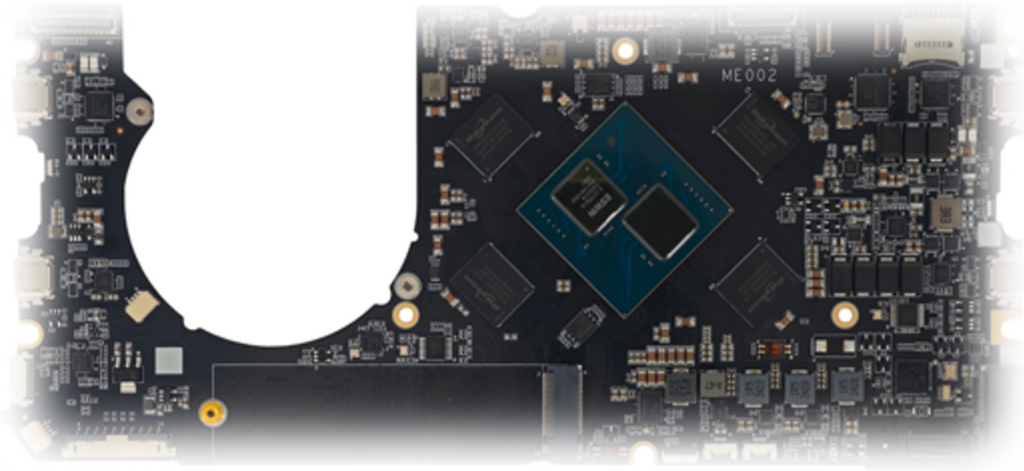
Framework RISC-V AI-PC Product Portfolio



Laptop 13” RISC-V (Professional)

- 8-12 Core 2GHz, <64G LPDDR5
- 50 TOPS AI Local Compute
- **June, $300+**

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Why Upstreaming

- RISC-V Business
  - Future NOT now， why?
  - Climbing Volume, why?

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Why Upstreaming

- Vendor Kernel
  - Endless Rebasing Effort
  - Endless Integration
  - Endless Question and Answer

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How to Upstream: A Painful Example

- JH7110
  - U74 SiFive IP: 2018
  - SoC: 2022
  - Product mainboard: 2024
  - Upstream
    - First PinCtrl: 9th Feb 2023
    - Last Display (DRM): still on going (stuck, Dec/2025)
    - Average Turn Around: 10+ resubmission

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How to Upstream: A Painful Example

- **Painfully Slow and Long Process**
- **Painfully Unpredictable**
- **Painfully No Future Business**
- **Something NOT right!**

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How to Upstream: Asking Advice

Linux Kernel Fellows Support

- See if Linus and Greg Help Speeding

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How to Upstream: Timing

Greg Kroah-Hartman

Fellow,

Linux Foundation

THE LINUX FOUNDATION

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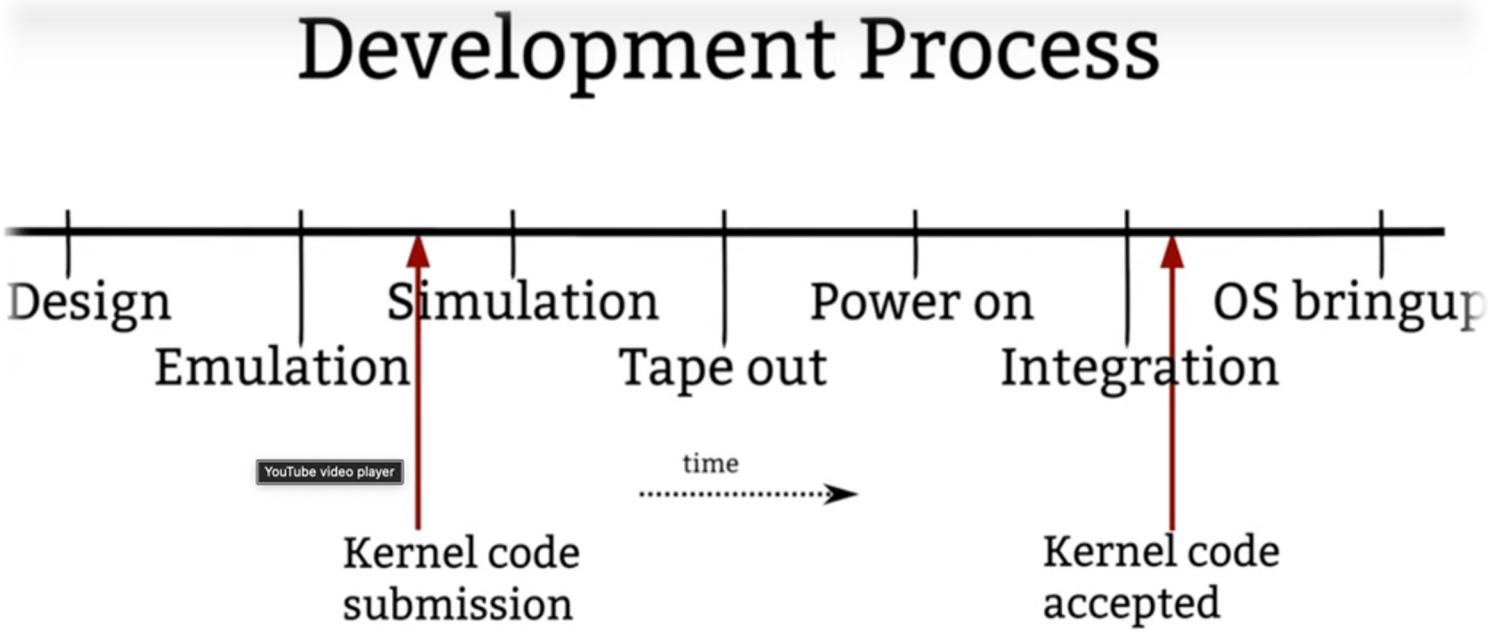
How to Upstream: Timing



Greg Kroah-Hartman

Fellow,

Linux Foundation

THE LINUX FOUNDATION

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How to Upstream: Pre-silicon

- Willingness Check
  - Hardware Close-Minded!!!
- Inheritance
  - Commonality
- Planed Order
  - Easy
  - Difficult
  - Virtually Impossible (Display)

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How to Upstream: Pre-silicon

- **Shift-Left As Much As Possible**
  - **Work on mainline**
    - **Backport to LTS**
  - **Pre-submission review for shorter turnarounds**
  - **Inviting Busy Maintainers**

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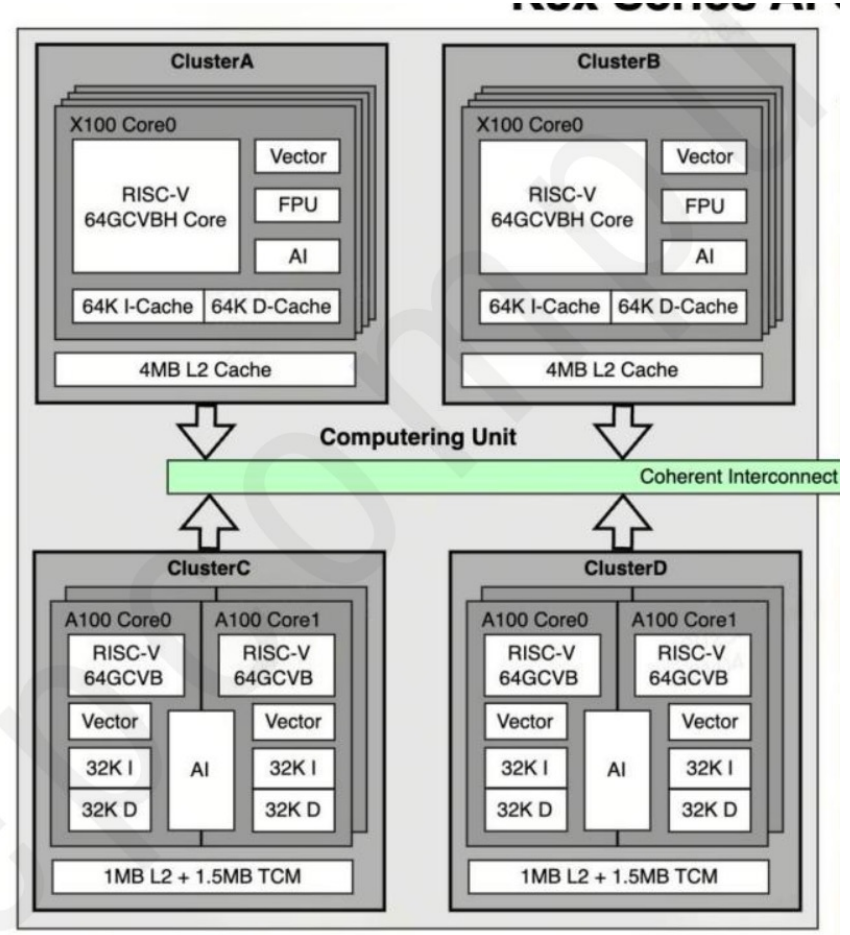
How to Upstream: Pre-silicon

- Any Surprises?
  - OMG, Asymmetric
    - RVA23 vs Non RVA23
    - RVV different vlen
  - OMG, PCIe
    - Not on 32bit DMA Zone
  - OMG, Public matters
    - Private Repository to Public
      - Avoid IP issues



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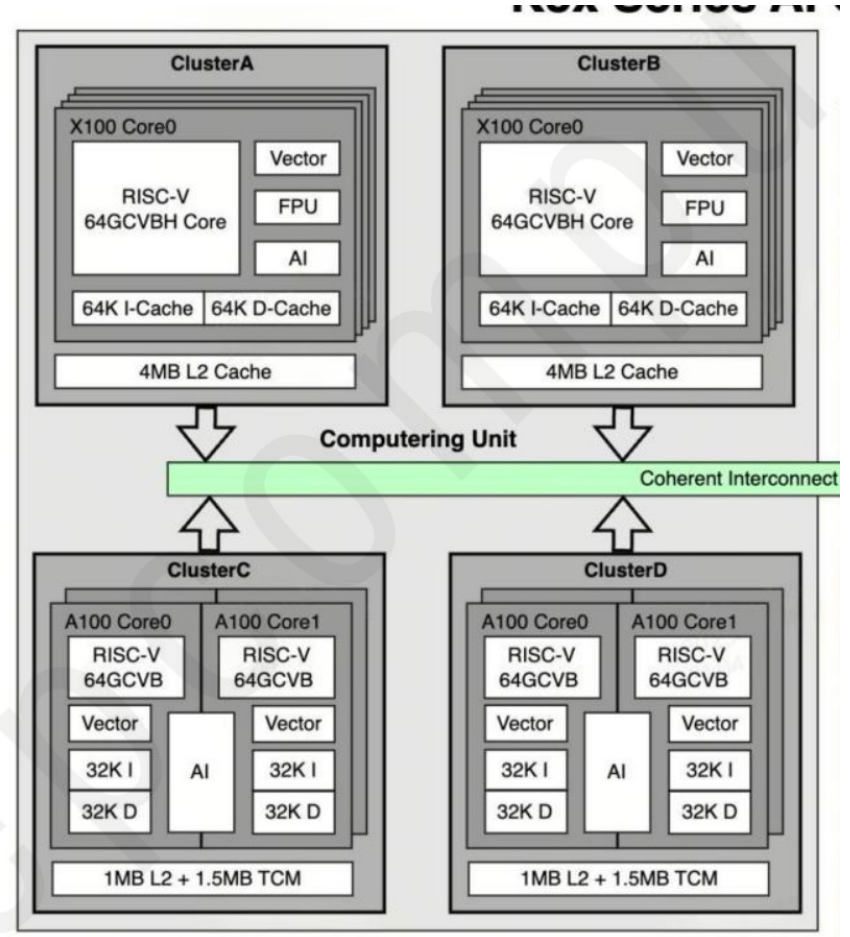
How to Upstream: Pre-silicon

- Breaking Rules?
  - FPGA target?
    - Short-life Target, NO!
  - Any Testing?
    - No Hardware!
  - Any Reputation Ruin?
    - What happen bugs!!



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What to Improve?

- Consider Upstream in Design Stage
- Consistent Design
  - With less Upstreaming effort in mind
- Be brave and not shy
  - Nothing more harmful than not upstreaming

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Thank You