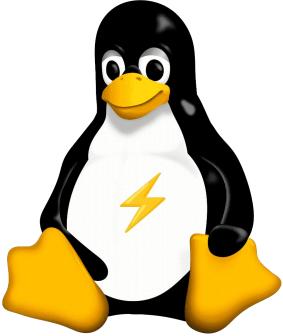
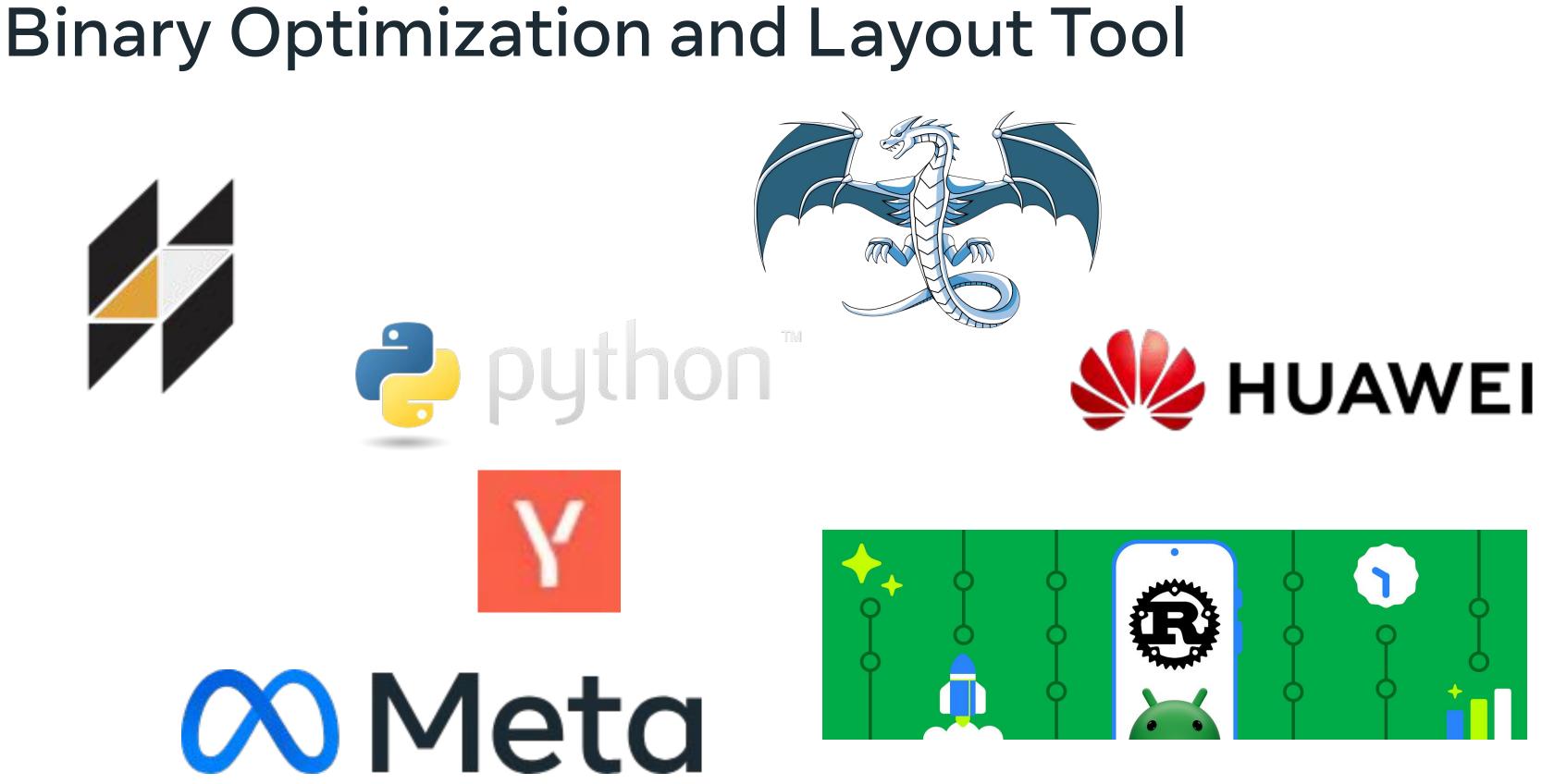
BOLT - Binary Optimizer for Linux Kernel

LINUX PLUMBERS CONFERENCE Vienna, Austria Sept. 18-20, 2024



Maksim Panchenko Meta, Inc



Agenda

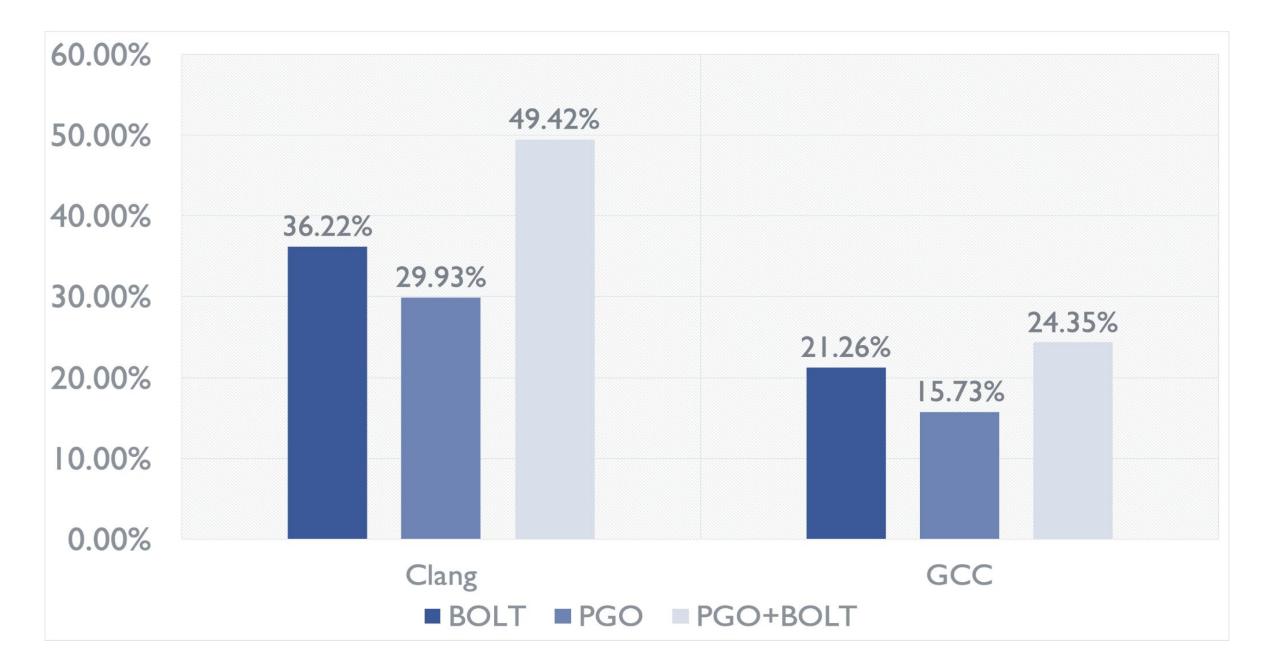
- 01 Introduction to BOLT
- 02 Kernel Performance
 - Numbers
- 03 Usage
- 04 Building Binary Optimizer
- 05 Linux Kernel Specifics
- 06 Advanced (Off)Topics

History

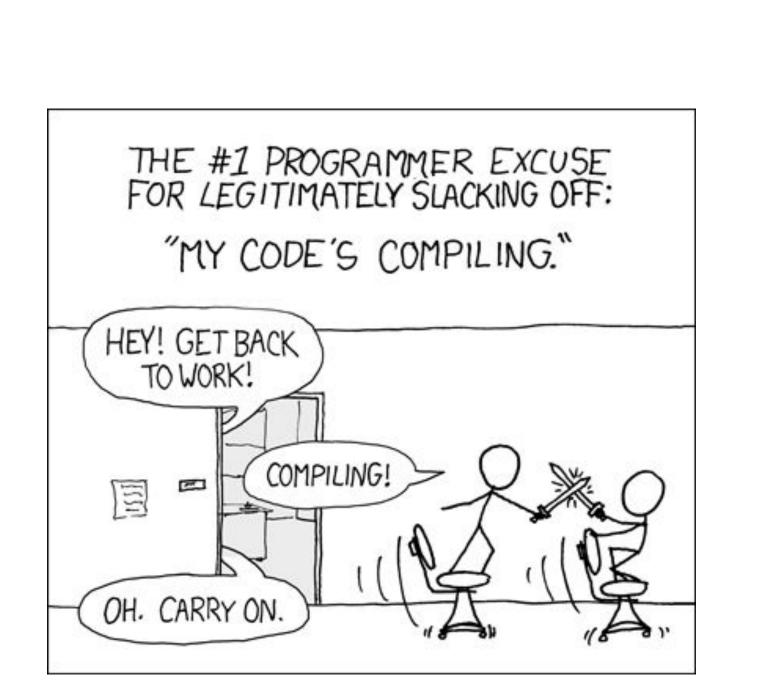
- $\circ~$ 10 years ago O3+PGO+LTO was the state of the art in the open source world
- 2015: conceived profile-based BOLT to work with any compiler toolchain
- $\circ~$ Double digit gains on top of compiler PGO+LTO
 - Speeding up both GCC and Clang
- Optimizing FB/Meta services since 2016
- Open-sourced since 2018
- $\circ~$ In LLVM since 2022

the open source world compiler toolchain

History



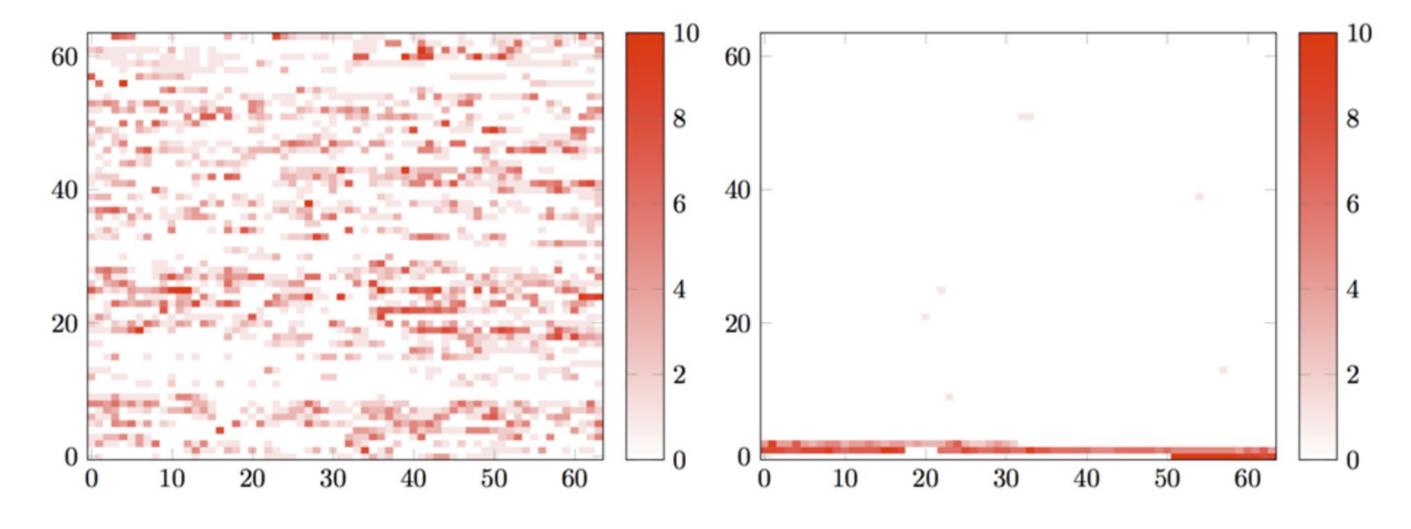
Why faster?



But How?

- Code Layout Optimizations
- L1 I\$ is small 32KB/64KB
- Compiler does not have enough information Ο
 - Inlining one of the reasons
- BOLT profiles at the lowest level Ο
 - Knows "final" edge profiles
- Two-stage PGO became de facto for *maximum* performance 0
 - "Large"/datacenter applications
 - **Context-sensitive PGO flavors** 0
 - More PLO tools

But How?



(a) without BOLT

(b) with BOLT

- Post-link Optimizer 0
- Part of LLVM project 0
- Complements compiler Ο
- Support popular architectures 0

- Post-link Optimizer 0
- Part of LLVM project Ο
- **Complements compiler** Ο
- Support popular architectures 0

Runs on ELF binary, e.g. *vmlinux*

0	Post-link Optimizer	 Runs
0	Part of LLVM project	 Runs
0	Complements compiler	
0	Support popular architectures	

on ELF binary, e.g. *vmlinux* on GCC-compiled code too

0	Post-link Optimizer	 Runs or
0	Part of LLVM project	 Runs or
0	Complements compiler	 PGO+L
0	Support popular architectures	

n ELF binary, e.g. *vmlinux* n GCC-compiled code too TO+BOLT for max performance

ns or
iO+Ľ

n ELF binary, e.g. *vmlinux* n GCC-compiled code too TO+BOLT for max performance

x86-64 AArch64 **RISC-V**

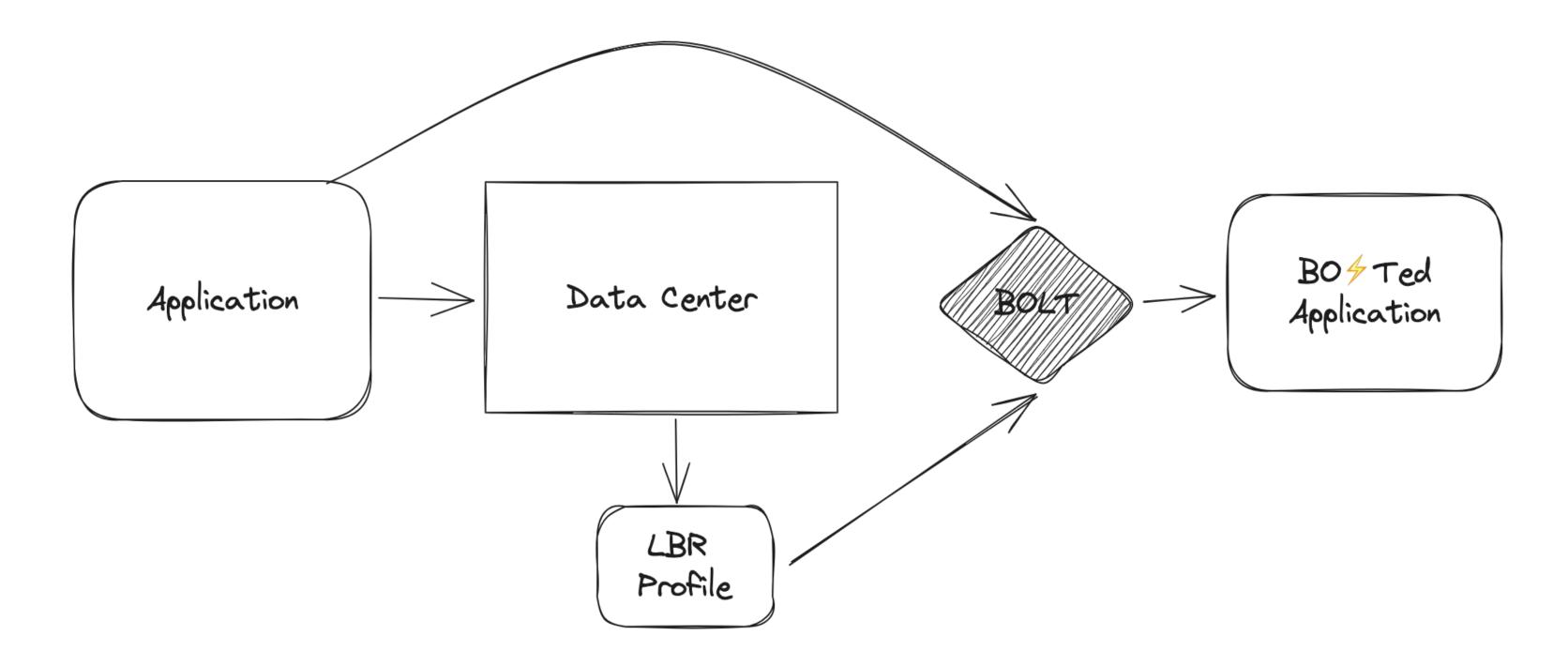
System Performance Improvements

- BOLT applied to the Linux kernel
- On top of PGO:
 - 2% QPS gain on Meta's TAO distributed data store
 - 2.5% gain on RockDB *db_bench fillseq*
 - ~30% reduction in *br_inst_retired.near_taken:k*
- Important considerations:
 - Kernel configuration
 - \circ $\,$ Time spent in the kernel
 - Micro- vs Macro- benchmark
 - System configuration and bottlenecks
 - \circ Quality of profile

BOLT Usage

- No recompilation required
 - Only if function splitting was enabled. BOLT splits better.
- Link with -q (-Wl,-q) a.k.a. --emit-relocs
- Takes seconds to optimize *vmlinux* 0

BOLT Usage Example



Profile

- Sampling branch data
 - *perf* with Intel LBR or similar
- $\circ~$ Instrumentation when LBR not available
- $\circ~$ Traces (PT or ETM)
- Cycles sampling

What does it take to build Binary Optimizer for Linux kernel?

 $\circ~$ Assumptions:

- $\circ~$ Well-formed unobfuscated code
- Compiler-generated code
- Assembly with good form
- Similar to *objtool?*
- Unstripped x86-64 ELF

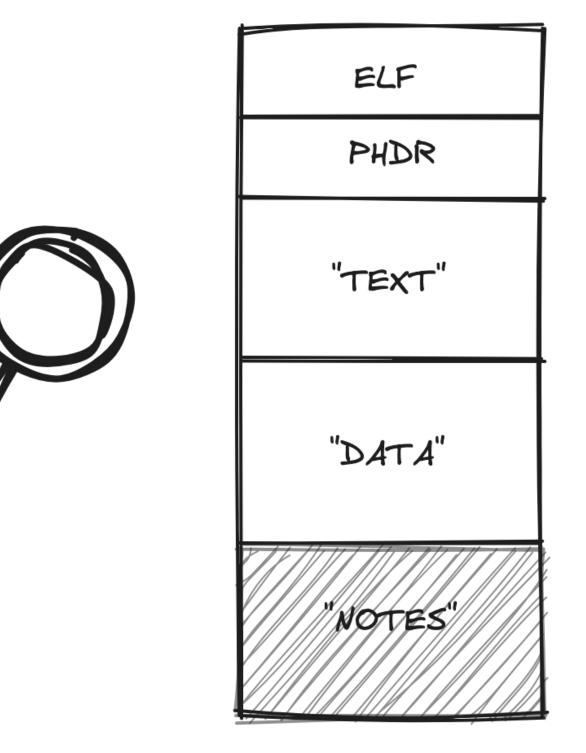
Building Binary Optimizer

Steps:

- Identify Code and Data
- Identify Functions and Boundaries
- Disassemble Functions
- \circ Build IR
- Attach Profile
- Run Optimizations
- $\circ~$ Emit and Write Optimized Code
- Update Metadata

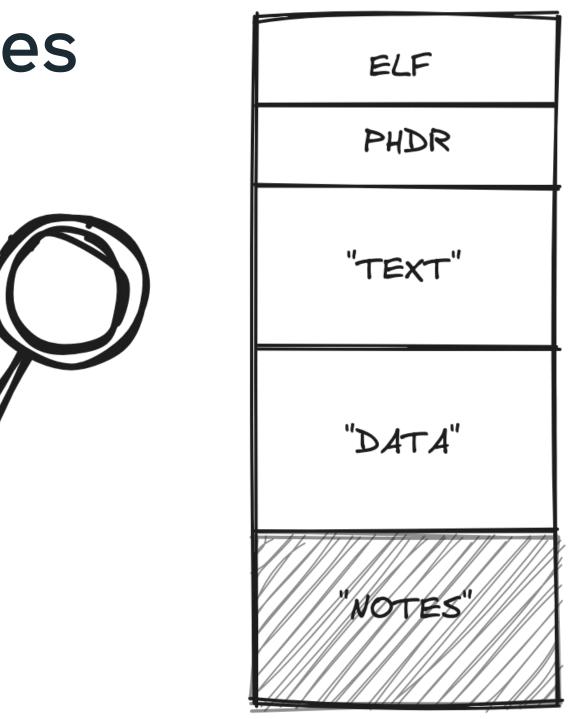
Identify Code and Data

- Segments
- \circ Sections
- \circ ELF flags
 - SHF_ALLOC | SHF_EXECINSTR
- Not a problem for unstripped binaries



Identify Functions and Boundaries

- Symbol Table
- Dynamic symbol table
- FDEs in *.eh_frame*
- Not a problem for unstripped binaries



Disassemble

- Symbolic disassembler
- How to distinguish constant from an address? 0
- x86-64 rip-relative addressing
- Linker relocations Ο
- Function pointers detection in code

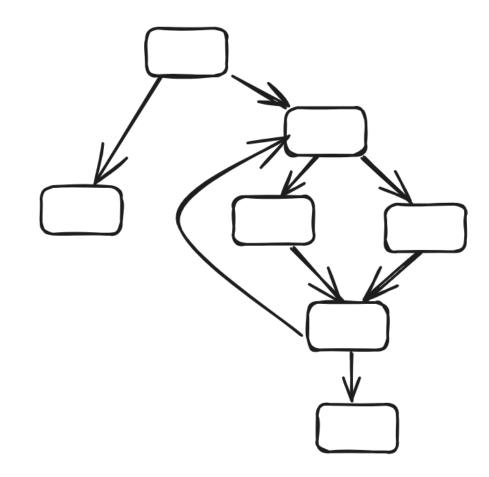
mova \$0x80000, Oxfaceb0 -> mova \$VAR, Oxfaceb0

Building Binary Optimizer

Build IR

- MCPlus
- LLVM MC-level instructions with annotations
- E.g. ORC annotations per instruction
 - Indicates frame/stack modification
- With CFG (basic blocks with edges)
- Leverage LLVM for low-level target analysis
- Challenge:
 - O Indirect jumps pusha %rbx # ORC: {s

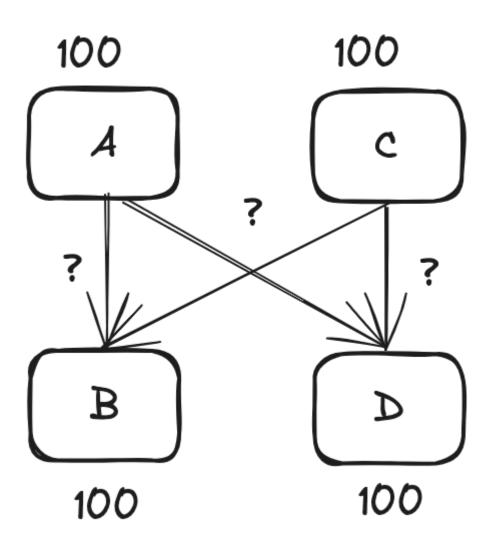
movq



%rbx # ORC: Esp: 8, bp: 0, info: 0x5} %rdi, %rbx # ORC: Esp: 16, bp: 0, info: 0x5}

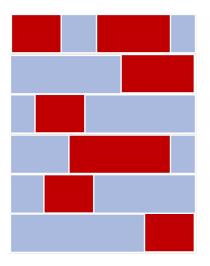
Attach Profile

- Profile on edges for optimal layout decisions
- \circ A \rightarrow B could be anywhere in [0, 100]
 - Optimal path for layout unknown
- $\circ~$ Without edge info, some info can be recovered

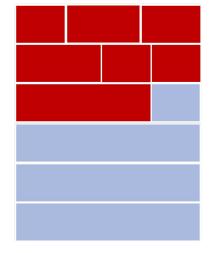


Run Optimizations

- Focus on Code Layout
- Basic-Block Reordering (ext-TSP)
- Function Splitting
 - $\circ~$ Hot/Cold is the basic
 - CDSplit
- Fragment/Function Reordering
 - \circ CDSort
- x86-specific branch optimization on hot path



Hot

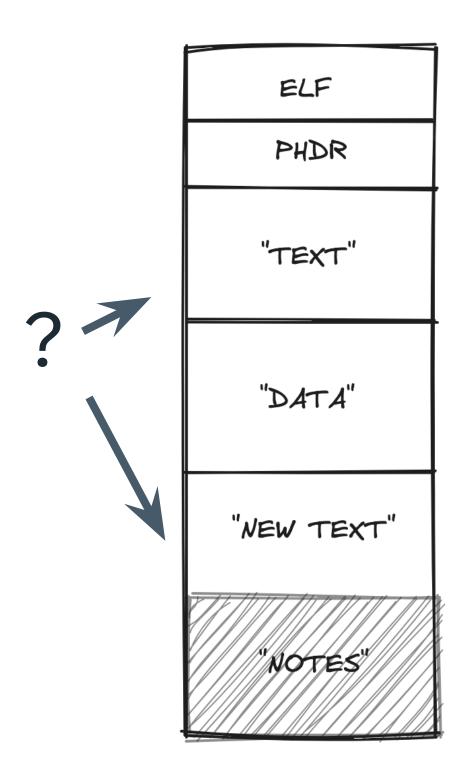




Emit and Write Optimized Code

No need to re-write data

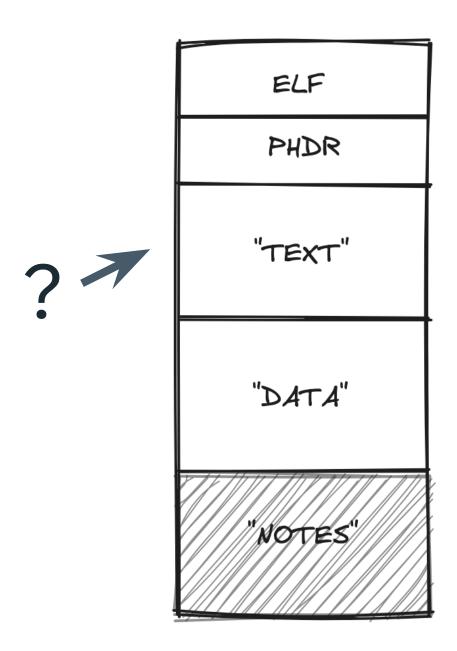
- Update code references
- Jump Tables
- \circ Where place new code?
 - Original function bodies
 - New segment
 - Reuse .text but erase old code first



Emit and Write Optimized Code

Update functions in-place

- \circ Safe
- $\circ~$ Works without relocations too
- Piggy-backs on compiler/linker function order
- Prevents over-specialization of code layout
- Brings most of performance benefits
- Con: suboptimal coverage



Update Metadata

- \circ Critical
 - $\circ~$ ELF and PHDR tables
 - o .eh_frame + .eh_frame_hdr
 - C++ exception table
 - Existing ranges are interrupted
- Less critical (but still important)
 - Symbol table
 - DWARF
 - Compiler pseudo probes
 - \circ etc.

Linux Kernel Metadata

- Sets kernel apart from user space
- Code modifications at boot time and runtime are common Ο
- What You See Is *NOT* What You Get Ο
 - w/ "objdump -d"
- Challenges for Binary Optimization

Linux Kernel Specifics

ORC

- Oops Rewind Capability
 - Similar to DWARF CFI but faster movq
- Optimized lookup tables
- Every instruction IP is virtually mapped to an entry
 - SPOffset
 - BPOffset
 - SPReg, BPReg, Type, Signal
- .orc_unwind + .orc_unwind_ip sections
 - .orc_lookup populated at runtime
- Every instruction annotated with ORC entry
- $\circ~$ Updated IPs for the new code layout
 - $\circ~$ Stack is unchanged

pusha %rbx # ORC: {sp: 8, bp: 0, info: 0x5} mova %rdi, %rbx # ORC: {sp: 16, bp: 0, info: 0x5}

SMP Locks

- *nop* or *lock* byte decided at boot time
- $\circ~$ Annotate instructions with "SMPLock"
- Update *.smp_locks* with new instruction addresses

lock # SMPLock: 1 and \$-0x21, (%rbx)

Static Calls

- Call instructions are updated at runtime
- Tracked by a table with entries:
 - s32 address
 - s32 key
- Annotate instructions with "StaticCall"
- Update addresses in the table
- Table sorted at runtime in *static_call_sort_entries(*)
 - Updates are in-place

____SCT____x86_pmu_read # TAILCALL # StaticCall: 11 # Count: 955 jmp

Static Keys

- NOP or JMP toggled at runtime
- Optimized for LIKELY case of static key, true or false
 NOP "most" of the time
- $\circ~$ The static keys table stores:
 - NOP/JMP location
 - *JMP* target
 - \circ Key info
- $\circ~$ Lower bit of Key indicates if the key is likely true
- Newer kernels optimize for *jmp* size (!)
- jump_label_update() updates all code entries for a key (batch mode)
- text_poke_bp_batch() overrides the first byte with int3

y (batch mode) t*3*

Static Keys

- BOLT recognizes code locations and adjusts CFG
- Special "conditional" branch *jit* (CC "it")

- BOLT optimizes for the final *JMP* size
- Can always output 5-byte *JMP* for compatibility
- $\circ~$ Update table with new addresses

Likely: 1 # InitValue: 0 :ount: 6553941)

Alternative Instructions: .alt_instructions

- Different instructions sequences depending on CPU features Ο
- Multiple alternatives possible Ο
- Alternatives can have their own ORC entries Ο
 - Same ORC table is shared putting restrictions on instruction boundaries (developers can use NOPs)
- Can include control flow instructions Ο
- BOLT annotates disassembly with alternatives Ο
- Hard to properly optimize unless CFG is fixed Ο

xsave64 (%rdi) # AltInst: "xsaveopt64 (%rdi)" # AltInst2: "xsavec64 (%rdi)" # AltInst3: "xsaves64 (%rdi)"

Paravirtual Instruction Table: .parainstructions

- Replaced by alternative instructions in new kernels
- Tracked by a table with entries:
 - \circ u8* instr
 - u8 type
 - \circ u8 len
- Annotate instructions with "ParaSite"
- \circ Skip optimization

Bug Table: <u>___bug_table</u>

- $\circ~$ Used for kernel debugging
 - WARN()/WARN_ON() & BUG()/BUG_ON()
- struct bug_entry
 - Pointer to *ud2* instruction corresponding to a bug
 - Always PC-relative on x86-64
 - Source location and flags
- Update *ud2* location
- o find_bug() uses linear search

ud2 # BugEntry: 181

Exception Table: ___ex_table

- Instructions that access user-space memory can cause page Ο faults
- The table references the memory instruction and the code where Ο the execution will resume.
- The table may be expected to be sorted Ο
- Currently BOLT skips functions with exceptions and fixups Ο

xsave64 (%rdi) # ExceptionEntry: 459 # Fixup: ___ENTRY_save_fpregs_to_fpstate@0xfffffff810390a6

PCI Fixup Table: .pci_fixup

- Lists code handlers for errors associated with a given PCI
- $\circ~$ BOLT verifies that handlers are at the start of a function
- \circ $\,$ No update needed $\,$

PCI

Kernel Metadata Summary

- All metadata can be dumped by BOLT 0
- BOLT Disassembly is annotated with Kernel metadata Ο
- Few changes between 5.19 and 6.8 Ο
 - E.g. *struct alt_instr*
 - BOLT automatically detects the correct data structure form
- Undetected Metadata?
 - Relocations pointing at function with displacement
 - Reject optimization

Not Covered in this Talk

- Profiling BOLTed Binaries
- Continuous Profiling
 - New source new binary
 - Binary Profile Inference
- Re-optimizing
 - Save original BOLT input
- Lightning BOLT
 - Parallel optimizations
- Other BOLT optimizations
- Security Applications

BOLT Run

BOLT-INFO: Target architecture: x86_64 BOLT-INFO: BOLT version: 149ea1e0524505349bbe195fb29cc0e3679b6401 BOLT-INFO: Linux kernel binary detected BOLT-INFO: first alloc address is 0x0 BOLT-INFO: static input executable detected BOLT-INFO: enabling lite mode BOLT-INFO: pre-processing profile using YAML profile reader BOLT-WARNING: function copy_user_enhanced_fast_string has an object detected in a padding region at address 0xffffffff818716d0 BOLT-WARNING: function __put_user_8 has an object detected in a padding region at address 0xffffffff81874b33 BOLT-INFO: parsed 13312 SMP lock entries BOLT-INFO: parsed 470 static call entries BOLT-INFO: parsed 1305 exception table entries BOLT-INFO: parsed 0 paravirtual patch sites BOLT-INFO: parsed 10684 bug table entries BOLT-INFO: setting --alt-inst-has-padlen=0 BOLT-INFO: setting --alt-inst-feature-size=2 BOLT-INFO: parsed 1200 alternative instruction entries BOLT-INFO: parsed 455063 ORC entries BOLT-INFO: parsed 865 PCI fixup entries BOLT-INFO: parsed 10716 static keys jump entries BOLT-INFO: 5657 out of 55728 functions in the binary (10.2%) have non-empty execution profile BOLT-WARNING: internal call detected in function __switch_to_asm BOLT-WARNING: internal call detected in function __switch_to_asm

. . .

• • •

BOLT Run

BOLT-INFO: basic block reordering modified layout of 3459 functions (61.15% of profiled, 6.21% of total) BOLT-INFO: 33 Functions were reordered by LoopInversionPass BOLT-INFO: program-wide dynostats after all optimizations before SCTC and FOP:

> 246560887 : executed forward branches (+5.3%) 15740399 : taken forward branches (-79.3%) 29878037 : executed backward branches (-29.5%) 10845129 : taken backward branches (-53.8%)

281608729 : total branches (-3.9%) 31755333 : taken branches (-72.7%) 249853396 : non-taken conditional branches (+41.2%) 26585528 : taken conditional branches (-73.3%) 276438924 : all conditional branches (-0.0%)

BOLT-INFO: the input contains 717 short and 694 long static keys jumps in optimized functions BOLT-INFO: written 722 short and 689 long static keys jumps in optimized functions BOLT-INFO: patched build-id (flipped last bit) BOLT-WARNING: Linux kernel support is experimental BOLT: 4885 out of 55728 functions were overwritten. BOLT-INFO: rewritten functions cover 74.72% of the execution count of simple functions of this binary

BOLT Disassembly

____traceiter_sched_process_free()

.Ltmp4523 (7 i	instructio	ns, align : 1)
Exec Count	: 1525	
Predecessors	s: .Ltmp452	23, .LFT3292
00000017:	mo∨q	(%rbx), %rax # ORC: {sp: 24, bp: 0, info: 0x5}
0000001a:	mo∨q	0x8(%rbx), %rdi # ORC: {sp: 24, bp: 0, info: 0x5}
0000001e:	mo∨q	%r14, %rsi # ORC: {sp: 24, bp: 0, info: 0x5}
00000021:	callq	*%rax # CallProfile: 1768 (942 misses) :
{b	of_trace_s	ched_process_template/1: 1768 (942 misses)
00000023:	cmpq	\$0x0, 0x18(%rbx) # ORC: {sp: 24, bp: 0, info: 0x5}
00000028:	leaq	0x18(%rbx), %rbx # ORC: {sp: 24, bp: 0, info: 0x5}
0000002c:		.Ltmp4523 # ORC: {sp: 24, bp: 0, info: 0x5}
Successors:	.Ltmp4523	(mispreds: 450, count: 629), .Ltmp4522 (mispreds: 0, co

p: 24, bp: 0, info: 0x5}

count: 1307)

BOLT Disassembly

enqueue_task()

Exec Count : Predecessors: 0000004a:	23112 .LFT27 <mark>jit</mark>	ons, align : 1) 37, .Ltmp4590 .Ltmp4592 # ID: 1275 # Size: 2 # Likely: 1 # InitValue: 0 # (2 (mispreds: 3, count: 23112), .Ltmp4588 (mispreds: 0, count: (
Exec Count : Predecessors: 0000004c: 00000053: 00000056: 00000059: 0000005c: 0000005f: 00000061: 00000063: { enque { enque	27838 .Ltmp4 movq movq movq movq movl popq popq jmpl ue_task	<pre>(%rax), %rax # ORC: {sp: 32, bp: 0, info: 0x5} %r15, %rdi # ORC: {sp: 32, bp: 0, info: 0x5} %r14, %rsi # ORC: {sp: 32, bp: 0, info: 0x5} %ebx, %edx # ORC: {sp: 32, bp: 0, info: 0x5} %rbx # ORC: {sp: 32, bp: 0, info: 0x5} %r14 # ORC: {sp: 24, bp: 0, info: 0x5} %r15 # ORC: {sp: 16, bp: 0, info: 0x5} *%rax # TAILCALL # ORC: {sp: 8, bp: 0, info: 0x5} # CallPro- _fair/1: 27458 (12320 misses) }, _rt/1: 1 (1 misses) },</pre>
{ enque	ue_task	_stop/1: 81 (81 misses) }

ORC: {sp: 32, bp: 0, info: 0x5} 0)

ofile: 27540 (12402 misses) :

BOLT Disassembly

read_tsc()

.LBB0101 (7 instructions, align : 1)					
Entry Point					
00000000:	<pre>rdtsc # AltInst: "lfence; rdtsc" # AltInst2: "rdtscp" # ORC: {s</pre>				
0000002:	<pre>nop # Size: 1 # AltInst: "lfence; rdtsc" # AltInst2: "rdtscp" #</pre>				
0000003:	<pre>nop # Size: 1 # AltInst: "lfence; rdtsc" # AltInst2: "rdtscp" #</pre>				
00000004:	<pre>nop # Size: 1 # AltInst: "lfence; rdtsc" # AltInst2: "rdtscp" #</pre>				
00000005:	shlq				
0000009:	orq %rdx, %rax # ORC: {sp: 8, bp: 0, info: 0x5}				
000000c:	retq # ORC: {sp: 8, bp: 0, info: 0x5}				

sp: 8, bp: 0, info: 0x5}
NOP: 1 # ORC: {sp: 8, bp: 0, info: 0x5}
NOP: 1 # ORC: {sp: 8, bp: 0, info: 0x5}
NOP: 1 # ORC: {sp: 8, bp: 0, info: 0x5}

Thanks! github.com/llvm/llvm-project/bolt

