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Type2 support: CXL.mem status and future CXL.cache

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As the author of a current RFC patchset under review for supporting a Type2 CXL device, it is worth to summarize what has been discussed so far, the current status of the patchset and also other tangential concerns like full privacy or CXL/PCIe slot resets and restoring CXL registers.

CXL.cache needs also to be discussed with the goal of defining a roadmap or at least first steps towards fully support, likely starting with security for restricting what a CXL.cache capable device can do. I will present a template for trying to define those goals.

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