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Shared FPU Support in Zephyr for ARM64 and RISC-V

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Computers are good at doing computations, obviously. But this is not that simple when floating point numbers are involved. Many processors implement a dedicated floating point unit (FPU) to perform computations on such numbers much faster compared to using the regular arithmetic logic unit (ALU).

FPU usage is not free though, especially when an operating system is involved whose purpose is to arbitrate resource usage amongst competing computing tasks. The FPU context may be quite large and simply preserving and restoring it across task switches, just like with the ALU context, may represent a significant overhead we want to avoid when possible, especially on an RTOS such as Zephyr. But adding smartness to the FPU context switching does come with its share of challenges and surprises.

In this presentation we'll quickly review the IEEE754 floating point standard in the context of ARM64's and RISC-V's FPU. Then we'll look in greater details at Zephyr's FPU sharing support for those architectures, design rationales, as well as some interesting snags the implementation had to deal with.

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