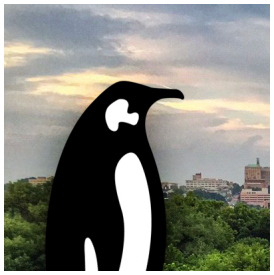

Contribution ID: **137** Type: **not specified**

Using hardware hints for optimal page placement

Wednesday, 15 November 2023 15:15 (45 minutes)

Hardware platforms have started exposing useful and actionable memory access information to the OS in various ways [1] [2]. There are sub-systems in the kernel like NUMA balancing which need such information but currently employ software methods to generate and act upon such access information. They could benefit if hardware can directly provide access information to the kernel in an easy to consume manner.

This talk intends to look at the ways, opportunities (NUMA balancing, reclaim, hot page promotion in tiered memory systems) and challenges in using hardware provided memory access information within the kernel. The talk will also share the experience of using the Instruction Based Sampling (IBS) mechanism present in AMD EPYC processors for NUMA balancing and hot page promotion.

[1] https://lore.kernel.org/linux-mm/20230208073533.715-1-bharata@amd.com/
[2] https://lore.kernel.org/linux-mm/20230402104240.1734931-1-aneesh.kumar@linux.ibm.com/

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