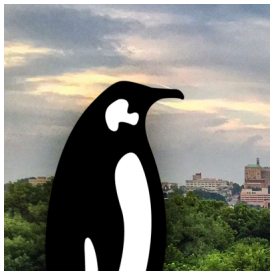

Contribution ID: **198** Type: **not specified**

Perf feature improvements in RISC-V

Monday, 13 November 2023 11:55 (15 minutes)

RISC-V Linux kernel has some basic perf support with counter overflow and stat until now. This has its own limitations and multiple perf related ISA extensions are being drafted to address these concerns. We would like discuss few of the existing challenges and new issues related to implementation for new ISA extensions. For example, counter event mapping, event encoding, host + guest usage for perf, kernel blind spot profiling with SSE, restricted user space access for cycle/instret.

The objective is to get an early feedback from the community to figure out the best path forward.

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Session Classification: RISC-V MC

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