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CXL Type-2 core support

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“Type-2” device support is made up of a series of new CXL features. Each of these features warrants some discussion on it’s own.

Features such as P2P, Back-Invalidate, Cache-ID configuration are all modifications to the core required by accelerator devices.

Dan Williams has already opened up the internal memory configuration to outside device drivers with his type-2 patch series. However, there are sure to be additional details which need to be ironed out when real devices start to be released.

I propose a session covering what support is currently upstream, what support is planned by my own work on type-2 devices (including qemu work), as well as what future work will be required. Audience participation will be encouraged, especially when discussing future work.

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