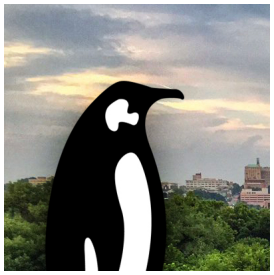

Contribution ID: **18** Type: **not specified**

RISC-V MC

We'd like to propose another edition of the RISC-V microconference for Plumbers at 2023. Broadly speaking anything related to both Linux and RISC-V is on topic, but discussion tend to involve the following categories:

- How to support new RISC-V ISA features in Linux, both for the standards are for vendor-specific extensions.
- Discussions related to RISC-V based SOCs, which frequently include interactions with other Linux subsystems as well as core arch/riscv code.
- Coordination with distributions and toolchains on userspace-visible behavior.

Likely Topics for Discussion Sections

The actual list of topics tends to be hard to pin down this early, but here's a few topics that have been floating around the mailing lists and may be easier to resolve real-time:

- Do we even bother with generic optimized lib routines, or just go vendor-specific?
- When can we start deprecating stuff? Likely-unused bits include: rv32, nommu, xip, old toolchains.
- Is it time to give up on profiles and just set a base ourselves?
- CI: Hosting PW-NIPA (currently hosted by Conor/Microchip), hosting "upstream kernel ci"on Github w/ sponsored runners?
- Hardware assisted control-flow integrity on RISC-V CPUs.
- Handling text patching on RISC-V systems.
- How do we deal with vendor-specific memory management?

Key Stakeholders

Apologies if I've missed anyone, but I've tried to list a handful of the people who frequently show up and help drive discussions at the RISC-V microconferences we've held at past Plumbers:

- Palmer, Atish, Anup, Conor, Bjorn: all regular attendees and key contributors/maintainers of various RISC-V related subsystems.
- Arnd, Conor, Heiko, Emil: There are many new SOC families showing up with RISC-V ports, and much of the new
- We usually have attendance from a handful of the arm/arm64/ppc/mips/loongarch contributors/maintainers, as we share a lot of code and thus find many cross-arch issues. There's probably going to be even more now that we've got many shared SOC families.
- Carlos/Nick: Due to the nature of RISC-V we end up with many complicated toolchain interactions, so it's always good to have some time to discuss toolchain topics.

Accomplishments post 2022 Microconference

All the talks at the 2022 Plumbers microconference have made at least some progress, with many of them resulting in big chunks of merged code. Specifically:

- The riscv_hwprobe() syscall has been merged. [1]

- Support for ACPI has been merged [2].
- Kconfig.socs is in the process of being refactored.
- Preliminary patches for the RISC-V TEE have been posted. [3]
- Some optimized routines have been merged, but
- Text patching is still up in the air, but we've been working through many of the issues pointed out during the discussions.

[1] https://lore.kernel.org/lkml/168201218504.13763.1031176103296142331.b4-ty@rivosinc.com/
[2] https://lore.kernel.org/lkml/168571802526.11683.10109882495660507850.git-patchwork-notify@kernel.org/T/#m63a10dffd4070de35c4
[3] https://lore.kernel.org/lkml/20230421153514.tpqzvdu7zt7pe7hs@amd.com/T/

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