Hardening Linux guest kernel for CC

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Why to harden?

VMM <-> Guest runtime interaction
- Paravirt (MSRs, PortIO, MMIO, CPUID, ...)
  - TDX specific hypercall (TDVMCALL)
  - DMA shared memory regions (i.e. virtIO)

- Big and distributed attack surface*
  - Applies to all Confidential Cloud Computing (CCC) technologies
  - Input handling complexity varies (simple bit reads ↔ complex struct parsing)
  - Surrounding code has not been specifically written to withstand a maliciously crafted input
  - A single bug can be enough to gain a read or write primitive inside a guest kernel

*5.11 + desktop config: 26371 distinct guest kernel locations (90% in drivers)
Device filter

**Problem:** Drivers are 90% of threat attack surface (see slide 2)
- Device drivers are not written with CC threat model in mind
- Too many to be able to harden/audit

**Solution:** Device filter: disable in runtime all devices except a pre-defined allow list
- Currently allow list for buses: pci, acpi, platform
- Current list of PCI authorized devices for TDX guest:
  - virtio-block, virtio-net, virtio-console, virtio-9p and virtio-vsock
- Command line option to extend allow list

**Alternatives?**
- Minimal CC guest kernel config?
  - Doesn’t fit vendor model of single distro config
  - Needs constant maintenance to make sure all devices are disabled
  - Not clear if it can disable all drivers, including platform drivers

**Upstream feedback (Greg):**
1. Should be done in driver core
2. Should take into account usb/thunderbolt cases
3. Allow list is better managed by userspace/initrd

**Current status:**
- 4 patches that address 1 & 2: [https://github.com/intel/tdx/commits/guest-filter-upstream](https://github.com/intel/tdx/commits/guest-filter-upstream)
- Aspect 3 still needs patch(es) created

**Opens:**
- Support for varied PCI IDs (NVMe direct assignment, ..)
  - Based on class: PCI_CLASS_STORAGE_EXPRESS?
  - Would class-based cover all generic cases?
- ACPI shared memory regions allocation
  - Many ACPI drivers don’t do ioremap calls by themselves, but use (via AML methods) OperationRegions declared in their AML objects
  - Changing ACPI core to automatically share all touched regions opens attack surface too much
Paravirt-based communication interfaces

**Problem:** these interfaces can be used as attack vector from host/VMM

- Device filter should cover most of attack surface, but
- Many drivers will consume host input already their init functions
  - 5.15-based TDX kernel: 198 unique \_init functions, 5198 unique code locations
    - pci config space: 83 unique \_init functions, 772 unique code locations
    - msrs & apic: 72 unique \_init functions, 91 unique code locations
    - rest is MMIO & port IO
- Data for 5.15-rc1:

Will cover now solutions for:
- MMIO & shared memory
- PCI config space
- Port IO

- See backup slides for details:
  - MSRs
  - CPUIDs
  - KVM hypercalls and KVM CPUIDs
MMIO & shared memory

MMIO

- MMIO from userspace is disabled
- Kernel MMIO: opt-in shared with VMM using ioremap_driver_hardened()
- Automatically for authorized pci drivers & MSI mailbox
- Code:
  - https://github.com/intel/tdx/commit/90bd3f
  - https://github.com/intel/tdx/commit/80888b76
  - https://github.com/intel/tdx/commit/a790083
  - https://github.com/intel/tdx/commit/16097a5
  - https://github.com/intel/tdx/commit/16b90c1

- Opens:
  - ACPI OperationRegion support is still open

Shared memory: VirtIO

- Only split virtqueue without indirect descriptor support
- No support for virtio-pci-legacy mode and virtio-mmio
- Payload data is untrusted and must be verified separately
- Code:
  - https://github.com/intel/tdx/commit/c39c252d6
  - https://github.com/intel/tdx/commit/3377879
PCI config space

- Only through CF8: MCFG config space is disabled
- PCI config space access is blocked from non-allowed devices
  - 1 patch: github.com/intel/tdx/commit/1507340

Opens:
- Hotplug support
Port IO & Port IO filter

- **Port IO filter:** small allow list of ports in #VE handler
  - Only early and normal port IO
  - No filtering in decompressed mode
  - RTC, PCI config space, ACPI ports
  - Code: [https://github.com/intel/tdx/commit/58ca3fe](https://github.com/intel/tdx/commit/58ca3fe)
  - Port IO from userspace is not supported

Opens:
- Having a hardcoded port list in kernel is likely not good
- Some ports might need to be open based on ACPI table configuration
ACPI & ACPI filter

Problem: ACPI tables can be used as an alternative attack vector
- In TDX case: ACPI tables are passed via TDVF and measured
- But what a safe configuration for all these 55+ tables?
  - Some tables, like DSDT, are complex, have many features, etc.
  - Most of them are not needed for CC guest

Solution: ACPI filter: minimal set of allowed ACPI tables
- XSDT, FACP, DSDT, FACS, APIC, SVKL, TDEL
- Command line option to extend the list
- Code:
  - https://github.com/intel/tdx/commit/4a120bb
  - https://github.com/intel/tdx/commit/6712f7b
  - https://github.com/intel/tdx/commit/a4239c1d2

Potential future work:
- Minimal ACPI configuration for CC guest
- Hardening of AML interpreter
Summary

- Hardening CC guest kernel applies to all CC solutions
- Core hardening mechanism are important to get right
- Only can be done as collaboration/partnership
  - Intel is ready to contribute, but we cannot do this alone

- What collaboration method is most effective?
  - Sending patches/doing discussions on coco mailing list vs lkml?
  - Once a month sync call with all the interested players to plan the work further?
References

- TDX guest hardening public documentation:

- Public Tools (audit & fuzzing):
  - [https://github.com/intel/ccc-linux-guest-hardening](https://github.com/intel/ccc-linux-guest-hardening)

- Patches:
  - [https://github.com/intel/tdx/tree/guest](https://github.com/intel/tdx/tree/guest) & other guest branches

- More detailed talk on CC guest kernel hardening aspects:

- Contact: [elena.reshetova@intel.com](mailto:elena.reshetova@intel.com)
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Backup
MSRs

- **Trusted**: TDX module controlled
  - **Disallowed**: #GP(0) or conditional #GP(0)
    - Examples: IS32_SMBASE, IA32_VMX_*, ..
  - **Native**: Context switch by HW
    - Examples: IA32_SPEC_CTRL, IA32_SYSENDER_*, IA32_FSBASE/GSBASE, ..
- **Untrusted**: TDX module inserts #VE or direct access via TDVMCALL
  - **Audit & Fuzzing**: Simple handling in code (bitmasking), pay attention to enabled features
  - **Disable complex and unneeded MSRs**: IA32_MTRR_*
    - IA32_MKTME_PARTITIONING, ..
CPUIDs

- **Trusted:** TDX module controlled
  - Configured per attested params: XFAM, ATTRIBUTES, TD_PARAMS, CPUID_CONFIG
  - Native and Fixed
- **Untrusted:** TDX module inserts #VE or direct access via TDVMCALL
  - Disable unneeded: X86FEATURE_CQM(LLC), X86FEATURE_MBA, X86FEATURE_TME
  - #VE handler only issues TDVMCALL for range 0x40000000 - 0x400000FF
KVM hypercalls & CPUIDs

- All untrusted:
  - TDX module inserts #VE or direct access via TDVMCALL
- Disable all hypercalls apart from KVM_HC_SEND_IPI
- Disable all CPUIDs apart from
  - KVM_FEATURE_NOP_IO_DELAY
  - KVM_FEATURE_PV_SEND_IPI
  - KVM_HINTS_REALTIME
- Code: 1 patch
  https://github.com/intel/tdx/commit/a768c6bea39012220ee5e0d8223636f59adbb5ff
Hardening strategy overview

Wide scale and targeted fuzzing to exercise the exposed attack surface either in-breadth or in-depth for more complex code locations

Attack surface minimization: enabled drivers, kernel subsystems, open I/O ports...

Static analyzer driven manual code audit to identify problematic places that might need to be disabled, target fuzzed or a code fix might be required

Iterative Approach
Hardening process for TDX guest code

**Audit**
1. Perform a smatch run on the target guest kernel source tree
2. Filter out code disabled by the driver filter
3. Perform manual audit of the results

**Fuzzing**
4. Run kAFL Fuzzer with several boot harnesses, collect code coverage and map to source (Qemu snapshot fuzzing + Intel PT trace dumps)
5. Cross reference generic code coverage against a list generated by smatch

**Diagram Details**
- **Input function list**
- **Guest kernel source tree**
- **smatch pattern**
- **List of findings**
- **Manual audit list**
- **safeguard trusted excluded wrapper**
- **Guest kernel**
- **kAFL agent**
- **Decode coverage**
- **Smatch list cross matching**
- **Host input points specific coverage info**
Results of hardening: 5.15-rc1

Audit tag distribution

<table>
<thead>
<tr>
<th>Audit results</th>
<th># code locations</th>
</tr>
</thead>
<tbody>
<tr>
<td>excluded</td>
<td>2505</td>
</tr>
<tr>
<td>wrapper</td>
<td>198</td>
</tr>
<tr>
<td>trusted</td>
<td>76</td>
</tr>
<tr>
<td>safe</td>
<td>1126</td>
</tr>
<tr>
<td>concern</td>
<td>81</td>
</tr>
</tbody>
</table>

Fuzzing coverage per audit tag type

<table>
<thead>
<tr>
<th>Audit tag type</th>
<th>% of code locations</th>
<th>% of functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>safe</td>
<td>86%</td>
<td>87%</td>
</tr>
<tr>
<td>concern</td>
<td>92%</td>
<td>100%</td>
</tr>
</tbody>
</table>

Stable reproducible fuzzing findings

<table>
<thead>
<tr>
<th>Fuzzing issue type</th>
<th># of bugs</th>
</tr>
</thead>
<tbody>
<tr>
<td>NULL pointer dereference</td>
<td>4</td>
</tr>
<tr>
<td>KASAN: user-memory-access</td>
<td>2</td>
</tr>
<tr>
<td>KASAN: out-of-bounds</td>
<td>7</td>
</tr>
<tr>
<td>kmalloc redzone oob</td>
<td>1</td>
</tr>
<tr>
<td>Supervisor write pagefault</td>
<td>2</td>
</tr>
<tr>
<td>Supervisor read pagefault</td>
<td>1</td>
</tr>
<tr>
<td>#GP</td>
<td>10</td>
</tr>
<tr>
<td>KASAN use-after-free</td>
<td>1</td>
</tr>
</tbody>
</table>

Existing functional patch fixes per area

<table>
<thead>
<tr>
<th>area</th>
<th># patches</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSIx</td>
<td>1</td>
</tr>
<tr>
<td>virtio-net</td>
<td>1</td>
</tr>
<tr>
<td>virtio-console</td>
<td>3</td>
</tr>
<tr>
<td>virtio-9p</td>
<td>1</td>
</tr>
<tr>
<td>virtio-pci-modern</td>
<td>1</td>
</tr>
</tbody>
</table>