ACPI support for RISC-V - Updates

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Agenda

- Platform requirements to support ACPI
- Engineering Change Requests (ECR) - status/plan for basic support
- Additional UEFI requirement
- Upstream process discussion
- Proposals for advanced features (WIP)
Platform requirements

1. **RV64** platforms, and
2. Advanced Interrupt Architecture (**AIA**) - IMSIC – Incoming MSI Controller
   - APLIC - Advanced Platform-Level Interrupt Controller (optional)
ACPI ECR status/plan

Batch 1 : Non-AIA (Under ASWG review)

Boot linux with SBI console, initrd

1. MADT RINTC V1 :
   - Per processor interrupt controller
   - ACPI processor ID and hartid association

2. RHCT : RISC-V Hart Capabilities Table
   - Timer frequency
   - ISA string - provides information about the extensions
ACPI ECR status/plan

Batch 2 : AIA + NUMA (Under RVI review)
1. MADT RINTC V2 :
   - Update with IMSIC base address/size
2. MADT – Add IMSIC and APLIC
3. APLIC device in the namespace
4. New RINTC affinity structure in the SRAT
Additional UEFI requirements

RISCV_EFI_BOOT_PROTOCOL
- Primarily to pass the boot hartid
- Ratified this year, UEFI spec is updated
- Support added in upstream u-boot and linux
- EDK2 support in progress
- Specification available [here](#)
Upstreaming linux patches

- Next version of ACPI spec would take at least an year even though ECRs get approved early

- ACPICA patches/ release
Features (WIP)

IOMMU support
- RISC-V IO Mapping Table (RIMT) specification

Power/Performance Management
- RISC-V FFH (Fixed Feature Hardware) specification
  - Required for LPI and CPPC
  - To be ratified and maintained within RVI
Acknowledgments

RISC-V Platform Runtime Services TG: tech-prs@lists.riscv.org

RISC-V Platform HSC: tech-unixplatformspec@lists.riscv.org

RISC-V OS-A-SEE Task Group: tech-os-a-see@lists.riscv.org
References

https://github.com/riscv-non-isa/riscv-acpi

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Thank You!
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Backup
Power / Performance Management

System sleep state management (_Sx states)
- Discovery of supported system sleep states - _Sx object
- Actual state transition through an SBI extension
Power / Performance Management

CPU idle state management (_LPI states)

- Support LPI (Low Power Idle) states for RISC-V
- Discovery of LPI states via _LPI objects
- State transition (entry method) via the SBI HSM extension
- FFH specification to transition to SBI call for the entry method
Power / Performance Management

- Support Collaborative Processor Performance Control (CPPC)
- Discovery of CPPC - _CPC object
- FFH spec for CPPC register access
  - Optional SBI extension