LINUX PLUMBERS CONFERENCE September 20-24, 2021

RISC-V Platform specification BoF

RISC-V Platform specification

- https://github.com/riscv/riscv-platform-specs/blob/main/riscv-platform-spec.adoc
- 2022 Platforms
  - OS-A Platform: This specifies a rich-OS platform for Linux/FreeBSD/Windows – flavors that run on enterprise and embedded class application processors
    - Base
    - Server Extension
- M Platform: This specifies an RTOS platform for bare-metal applications and small operating systems running on a microcontroller
  - Base
  - Physical Memory Protection (PMP) Extension
- Schedule
  - Frozen version 1.0 targeted by RISC-V Summit - Dec 2021

RISC-V ISA specification status

- Specification frozen (in public review phase)
  - H
  - V
  - SvPBMT
  - CMO
  - Sscofpmf

RISC-V non-ISA specifications

- RISC-V Profile
  - Krste, Andrew, Greg and others are working on this
- EBBR specification (Already released with RISC-V sections)
- UEFI specification (Already released with RISC-V specification)
- ACPI specification
  - As per the initial feedback from the distros, ACPI should be mandatory for server platforms
- Interrupt controller specifications
  - ACLINT – Frozen
  - PLIC – Frozen
  - AIA – Will be frozen soon (Anup ??)
- SBI specification (v0.3 is already frozen)

Open Questions - I

- Getting feedback from the distros
  - Feedback meeting with Canonical (Done)
  - Feedback meeting with RedHat (scheduled next week)
  - Feedback meeting with Suse (scheduled next week)

Open Questions - II

- How do we make RISC-V platform specification mandatory ?
  - “OS-A platform compatible” branding will be only issued that is compatible with the specification
  - Will the vendors care about the branding ?
- Platform compatibility test suite (PCT)
  - Still in discussion phase
  - Any ideas ?
    - Self certification of Linux booting ?
    - UEFI SCT/FWTS ?
    - A Kconfig option in a way that compatible platforms boot
    - Common SystemReady program for ARM64 & RISC-V ?
      - Dong from SystemReady is interested

To support D1 in upstream or not!

- Allwinner D1 incompatible with privilege specification
  - It uses two reserved bits even after Svpbmt is merged
  - Can it be considered as an errata ?
  - Does it setup a bad precedent and open can of worms in future ?
  - Can we allow this as an exception ?
    - Explicitly specify this board as an exception because the policy was not in place during the design phase
    - Any other way ?
  - Can we just ignore D1 given the mass volume ?

custom PBMT in D1 for non-coherency SOC