

Userspace synchronisation for asynchronous hardware engines

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Both future hardware and also user-visible APIs, are demanding that we discard our previous fence-based synchronisation model and allow arbitrary synchronisation primitives similar to Windows/DirectX 'timeline semaphores'. Outline the problems in trying to integrate this with our previous predictable fence-based model with `dma_fence` and `dma_resv` and discuss some potential paths and solutions.

I agree to abide by the anti-harassment policy

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Session Classification: GPU/media/AI buffer management and interop MC